Demonstration of High Power Density kW Converters utilizing Wide-Band Gap Devices

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DEMONSTRATION OF HIGH POWER DENSITY KW CONVERTERS UTILIZING WIDE-BAND GAP DEVICES

BY
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Demonstration of High Power Density kW Converters utilizing Wide-Band Gap Devices

Ph.D. Dissertation

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Curriculum Vitae

Nicklas Christensen

Nicklas Christensen received a B.Sc. degree in Energy Engineering with electrical specialization, from Aalborg University in 2014. In 2016 he received a M.Sc. degree in Power Electronic and Drives from Aalborg University. He is currently pursuing a Ph.D. degree within converter design using wide band gap devices at Aalborg University. During the PhD period an external stay at Danfoss Drives in Denmark was conducted. His research interest includes converter system optimization, wide band gap devices and electrical simulations using FEM software.

Abstract

Power electronic converters plays a key role in a wide range of applications, currently experiencing a rapid growth, such as energy generation, electric vehicles, electrical drives, data centers and portable electronics. Throughout the history of power electronics a continuous focus have been on optimizing the efficiency and power density to reduce physical size, weight and power losses. The reduction in size and increase in efficiency both implies a reduction in relation to manufacturing or operation cost of the converter. The advancement in efficiency and power density has been enabled by the development of new and improved semiconductor materials/devices. The next big advancement of power electronic converters are expected to be the newly emerging wide bandgap semiconductor devices, providing superior reductions in losses for the same blocking voltage. The main topic of this thesis is building converters with a high power density and efficiency, using the new wide bandgap devices. The major objectives of the thesis is to identify the performance limiting components and to optimize the converter on a system level. This involves selecting a suitable topology and design parameters, develop and optimize the converter layout digitally and performing experiments to evaluate on the performance obtained.

Chapter 1 introduces the background and motivation of the thesis. The chapter describes the continuous focus on power density and efficiency throughout the history of power electronics. Chapter 1 also introduces the new wide bandgap devices and the substantial advantages they introduce, together with the reinforced challenges appearing, when dealing with the faster switching devices.

Chapter 2 covers the disassembly of a commercial available power electronic product, to quantify the volume contribution of the major components. The disassembly of the converter guides the focus of optimization towards the filter and heatsink volume. Th filter and heatsink volumes are linked to the power dissipation from the power module and filter components. Chapter 2 is finished by reducing the potential topologies, based on state of the art research literature.

Chapter 3 present the design of an optimization algorithm based on the multi objective optimization algorithm named Pareto. The Pareto algorithm quantifies efficiency, power density and cost for a full inverter system. The inverter system includes DC-link capacitor, power module, gate driver, heatsink and output filter. The algorithm creates a large solution space of converter designs with different switching frequency, semiconductors and output filter inductors. As a results, a pareto front was created for each topology, presenting the optimum designs for each topology.

Chapter 4 present the simulation of a 10 kV SiC half bridge converter using finite element software, and the experimental validation of the parasitics extracted. The pur-

pose of the experiment was to validate the use of finite element software in performing digital design iterations. Due to the high dV/dt introduced by 10 kV SiC MOSFETs, the parasitic capacitive couplings were investigated. The capacitive network of the power module and heatsink were extracted and the behaviour was simulated. Comparing the waveforms obtained from simulation and experiment, a perfect agreement was observed. The perfect agreement validates the understanding of the power module and the accuracy of the finite element software, confirming its usefulness in a digital design process.

Chapter 5 present the initial design of the T-type power module, power routing and gate driver PCB. During the design process the size of the layout and its components are quantified, identifying a new power density limiting component. For a multilevel converter operating with a high switching frequency, a substantial volume contributions is introduced, by the increased number of gate drivers circuits. To reduce the size of the gate driver circuits, a novel bootstrap power supply was proposed. The conventional method of calculating the limitations of a bootstrap circuit, relies on rule of thumb estimations. A new method was as a consequence developed to accurately determine the modulation index limits. The improved method for calculating the limitations was used to evaluate the novel bootstrap circuit. The proposed bootstrap circuit for a T-type converter reduces the DC/DC converters count from seven to four, for a three phase converter.

Chapter 6 presents the development of the digital model and the experimental validation of it. A digital model was developed for the T-type converter including semiconductor models, impedance of the output filter, power module, power routing and gate driver parasitics. Optimum component selection and digital design iterations were performed based on the digital model. The performance obtained was validated experimentally, by performing a double pulse test. The double pulse test confirmed that clean switching was obtained without voltage overshoot. A deviation between the measured and simulated turn on was observed. By performing a root cause analysis of the potential cause of deviation, the most likely candidate was identified to be discrepancies between the IV-characteristics of the semiconductor model and the physical device.

Chapter 7 present the simulation and experiments of the full three phase T-type inverter. The simulation model is based on extracted information from the complex local simulations developed in chapter 6 and a thermal network extracted using COMSOL. The model of the full converter system, enabled the simulation of junction temperature and filter response during several fundamental output cycles. The system simulation was experimentally validated by comparing the measured and simulated inductor current ripple, presenting perfect agreement. The overall performance of the T-type inverter was validated by measuring the frequency content of the output current, showing high attenuation of the switching frequency harmonics. The three phase converter obtains sinusoidal output voltages and currents with only a $60cm^3$ filter per phase.

Chapter 8 concludes the thesis by combing the conclusions from each chapter.

Resumé

Effekt elektronik spiller en essentiel rolle i en lang række af applikationer, som oplever en hurtig udvikling, som for eksempel energi produktion, elektriske køretøjer, elektriske drev, data centre og småt elektronik. Gennem effekt elektronikkens historie, har der været et konstant fokus på at optimere effektiviteten og effekttætheden, for at reducere den fysiske størrelse, vægten og de elektriske tab. En reduktionen af størrelsen og en højere effektivitet medfører en reduktion i produktions- eller driftsomkostningerne for konverteren. Fremskridtene i forhold til effektiviteten of effekttætheden er opnået gennem udviklingen af nye og forbedrede halvleder materiale/komponenter. Den næste store udvikling inden effekt elektroniske konvertere forventes at være de nyankommne wide bandgap halvleder, som bidrager med markante reduktioner i elektriske tab for den samme blokeringsspænding. Denne afhandling fokusere hovedsageligt på at bygge konvertere med høj effekttæthed og effektivitet, ved hjælp af de nye wide bandgap halvledere. Afhandlingens hovedopgaver er derfor, at identificere de komponenter der begrænser udviklingen og optimere konverteren udfra en system betragtning. Dette indebære at vælge en passende topologi og design parametre, udvikle og optimere konverter layoutet digitalt og at udføre eksperimenter for at evaluere på ydeevnen opnået.

Kapitel 1 introducere baggrunden og motivation for afhandlingen. Kapitlet beskriver det vedvarende fokus på effekttætheden of effektiviteten gennem effekt elektronikkens historie. Kapitel 1 introducere også wide bandgap halvledere og de markante forbedring de introducere, sammen med de forstærkede udfordringer, der kommer med hurtigt reagerende halvledere.

Kapitel 2 dækker adskillelsen af et kommercielt effekt elektronisk produkt for at kvantificere fordelingen af volumen, blandt de store komponenter. Adskillelsen af konverteren styrer fokusset mod at reducere filterets og køleladens volumen, som er forbundet med effekt afsættelsen i power modulet og filter komponenterne. Kapitel 2 afsluttes med at indskrænke udvalget af potentielle topologi, ved hjælp af den nyeste forskning publiceret.

Kapitel 3 præsentere design processen af en optimering algoritme, baseret på Pareto, en optimerings algoritme med flere mål. Pareto algoritmen kvantificere effektiviteten, effekttætheden og prisen for et helt inverter system. Inverter systemet indeholder DC-link kondensatorer, power moduler, gate driver, køleplader og udgangs filtre. Algoritmen genere en stor mængde mulige konverter designs med forskellige udgangsfiltre, halvledere og switch frekvenser. Resultatet af optimerings algoritmen er en Pareto front, for hver topologi, som præsentere de optimal designs for netop denne topologi.

Kapitel 4 præsentere simuleringsmodellen af en 10 kV SiC halvbro konverter, som benytter sig af finite element software. De parasitiske værdier fra finite element softwaren bliver eksperimentelt valideret. Formålet med eksperimentet var at validere brugen af de parasitiske værdier i en digital design proces. På grund af de høje dV/dt introduceret af 10 kV SiC MOSFETs, er de kapacitive koblinger undersøgt. Det kapacitive netværk mellem power modulet og kølepladen blev udtrukket, og netværkets respons blev simuleret. En perfekt overensstemmelse blev observeret mellem simuleringen og de eksperimentelle forsøg. Den perfekte overensstemmelse validere både forståelsen af power modulet og præcisionen af finite element softwaren. Validering bekræfter dermed også brugbarheden af finite element software i den digitale design proces.

Kapitel 5 præsentere det første design af et T-type power modul, strømførende PCB og gate driver PCB. I forbindelse med design processen blev størrelsen af alle layouts og deres komponenter kvantificeret, hvorved en ny komponent blev identificeret til at være den begrænsende faktor for effekttætheden. For multilevel konvertere med høje switch frekvenser, vil antallet af gate driver kredsløb bidrage med en betydelig del af systems volumen. For at reducere størrelsen af gate driver kredsløbene, er en ny bootstrap strømforsyning forslået. Den konventionelle metode brugt til at beregne begrænsningen for modulation indekset afhænger af tommelfinger estimater. En ny metode er derfor udviklet for præcist at beregne begrænsningen for modulation indekset. Ved brug af den nye metode er begrænsningerne for det nye T-type bootstrap forsyning beregnet. Det foreslåede bootstrap kredsløb for en T-type konverter reducerer antallet af DC/DC konvertere fra syv til fire, for et tre faset system.

Kapitel 6 præsentere udviklingen af en digital model og dens eksperimentelle validering. En digital model er udviklet for T-type konverteren som inkludere halvleder modeller, impedanser for udgangsfiltre og parasitiske impedanser fra power modulet, gate driver og det strømførende PCB. De optimale komponent valg og design iterationer er foretaget, baseret på den digitale model. Ydeevnen opnået af konverteren er valideret eksperimentelt, ved udførelsen af en double pulse test. Double pulse testen bekræftede at en ren switching transient er opnået uden at introducere oversving i spændingen. En uoverensstemmelse mellem målte og simulerede kurver under tænding af halvlederne blev observeret. En undersøgelse af hovedårsagen til afvigelsen blev foretaget, hvor variationen mellem målte og simulerede IV-karakteristikkerne for halvlederne blev identificeret som den sandsynlige årsag.

Kapitel 7 præsentere simuleringsmodellen og eksperimenterne for den fulde tre fasede T-type inverter. Simuleringsmodellen er baseret på informationerne fra de komplekse lokale simuleringsmodeller i kapitel 6 og det termiske netværk, udtrukket fra COMSOL. Modellen af hele konverter systemet tillader en simulering af junction temperaturen og filter responset, over adskillige fundamental udgangscyklusser. System simulering blev eksperimentelt valideret ved at sammenligne den målte og simulerede strøm varians i spolen, som vidste en perfekt overensstemmelse. Den overordnede ydeevne af T-type inverteren blev valideret ved at måle frekvens indholdet af udgangsstrømmen, som vidste en høj dæmpning af det harmoniske indhold

introduceret af switch frekvensen. Den tre fasede konverter opnår derved sinusformet udgangsstrøm og spænding med et kun 60cm^3 filter.

Kapitel 8 konkludere afhandlingen ved at kombinere konklusionerne fra hvert kapitel.

Preface

The work performed in relation to the thesis is a part of two research projects at Aalborg University (AAU), Aalborg East, Denmark. The two projects are Intelligent Efficient Power Electronics (IEPE) and Advanced Power Electronics Technology and Tool (APETT). I am very thankful for the financial support provided by the Innovation Fund Denmark and the Department of Energy technology, enabling my Ph.D. study.

I would like to express my gratitude to my supervisor Prof. Stig Munk-Nielsen for his valuable guidance and motivation throughout my Ph.D. study. I would also like to thank him for giving me the opportunity to become a part of a research team and environment.

I would also like to thank my co-supervisors Assoc. Prof. Christian Uhrenfeldt and Assoc. Prof. Szymon Beczkowski for their continuous support, guidance and technical sparring. I am truly grateful for their support in not only improving my publications and Ph.D. thesis, but also in strengthening my ability to perform research.

I would also like to express my sincere gratitude to Radu Dan Lazar, Brian Beck Christensen, Andreas Aupke and Niels Gade from Danfoss Drives. Their continuous support, technical discussions and guidance has been a key element to solve many technical challenges appearing throughout my Ph.D. studies. Furthermore the friendly atmosphere they creating during my stay at Danfoss Drives, made me feel very welcome which i truly appreciate. I would like to thank Radu Dan Lazar in particular for the additional support he provided me, by programming the DSP and assisting me in performing experiments on the three phase converter system.

I would also like to thank my friends and colleagues for their friendly companionship and continuous support throughout my Ph.D. studies. In particular i would like to thank Dipen Narendra Dalal for his willingness in participate in technical discussions in addition to providing friendly encouragement throughout my Ph.D. studies.

I am also very grateful for the support, understanding and patience provided by my family and girlfriend throughout the years. Without their unconditional support, none of my achievements would have been possible.

Nicklas Christensen Aalborg University, August 2019.

Contents

CHAPTER 1

Introduction

This chapter presents the background and motivation of the thesis, followed by the objectives and its scientific contributions.

1.1 Background and motivation

Power converters are utilized in a wide range of applications, as for example in harvesting renewable energy, electrical transportation or in data centers which all are fields currently that experience rapid growth in installed capacity [1]. In these applications efficiency, power density and production cost are often the main objectives for optimization. Efficiency is an important performance parameter for better utilization of renewable energy sources, reduction of operation cost and increase of reliability. The power density of converters is likewise heavily prioritised and have been continuously increasing since 1970. The power density of converters are doubled approximately every 10 years [2]. The increase of power density is obtained by the advancement of power semiconductors, enabling an increase in the switching frequency. The switching frequency reduces the size of passive components in filters [3]. The Silicon technology used today is limited by the relative large losses associated with the switching of semiconductors. The high power dissipation results in high device temperatures and large heatsinks, limiting the obtainable switching frequency. The result of a low switching frequency are bulky input and output filters, contributing with a large weight and volume. The state of the art advancement of semiconductors is the utilization of wide bandgap materials such as silicon carbide (SiC) and gallium nitride (GaN) [4],[5]. The wide bandgap semiconductors allow for a significant decrease of switching and conduction losses when comparing to silicon (Si) devices with the same voltage blocking capability [6], [7]. The reduced losses allow the designer to increase the converter switching frequency and thereby significantly improve power density and efficiency [8],[9]. The reduced semiconductor losses, introduce new challenges in regards to signal fidelity, EMI, physical layout and the possibility of performing non-invasive measurements [10].

This thesis deals with the design process, challenges and the experimental validation of high efficiency, high power density converters utilizing wide bandgap technology.

1.2 Objectives of the thesis

The objective of the thesis is to develop a framework for designing and building high power density converters using the new fast switching wide bandgap devices.

- Determine the optimum topology, switching frequency and components using an optimization algorithm. The optimization objectives are power density, efficiency and cost.
- Design a converter layout and develop a simulation of the electrical performance using parasitics from 3D models.
- Evaluate the validity of parasitic extraction from a 3D model using experimental measurement.
- Evaluate and optimize converter layout based on important performance criteria.
- Perform experimental measurements of the converter prototype to validate and evaluate on digital models and design tools developed.

1.3 Contribution of the thesis

- Identification of the main components contributing to the volume of a converter, and the limiting factors for obtaining a higher power density.
- Proposes a method of selecting the optimum design parameters for converter using wide bandgap devices, based on analytical equations.
- Establish a method for generating an accurate digital representation of a converter, without the need of a physical prototype
- Identifying and validating performance of critical design loops, when utilizing fast switching devices.
- Demonstrating a high performance SiC power module, by carefully considering the layouts and its parasitic contribution
- A new bootstrap circuit is proposed to reduce the volume and cost of gate drivers for multilevel converters, while achieving a high modulation index.
- Demonstration of significant power density and efficiency improvement for a converter system by utilizing wide bandgap devices.

CHAPTER 2

State of the art

2.1 Review of Existing Products

To realize the goal of significantly increasing the converter power density, an investigation of the current state of the art frequency converter and its volumetric distribution is required. A disassembly of commercial converter products will provide a foundation by providing knowledge about the level of commercial development. The knowledge gained from existing converter products will aid to guide the research focus, enabling a high degree of synergy between industry and research. The disassembly of a Danfoss 3 kW variable frequency drive is therefore performed [11]. The disassembly of the variable frequency converter was performed by mapping the volumetric size of its major components. A principal schematic of the variable frequency converter is shown in figure 2.1 representing the three categories of common and differential mode filter, DC-link and rectifier/inverter.

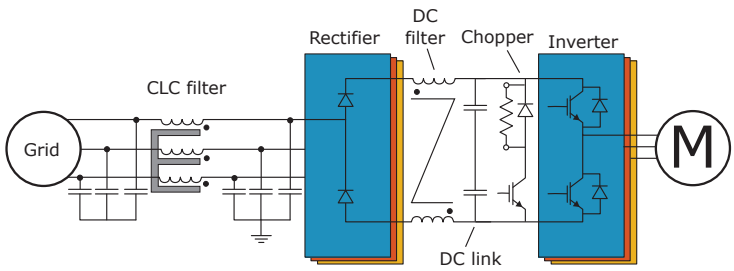

Figure 2.1: Principal converter schematic of Danfoss VLT AutomationDrive, FC 302.

The different components are sorted in categories based on their fundamental function. The filter contains the common mode CLC filter and the differential mode DC line filter. The rectifier/inverter category contains the rectifier, inverter and chopper excluding the resistor. The resistor is excluded due to it being externally connected through output terminals of the converter. The DC-link is consisting of two electrolytic capacitors each with a voltage rating of 450 V, serial connected to withstand the full DC-link voltage. Adding additional categories such as control and cooling, a pie chart describing the volumetric size of the major component is realised as shown in figure 2.2

What becomes evident from figure 2.2 is the rectifier/inverter accounts for only

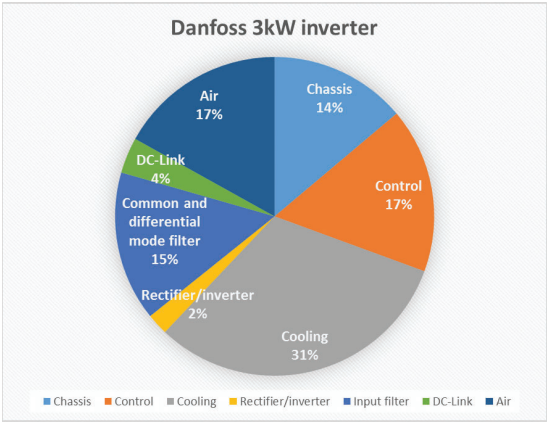

Figure 2.2: Pie chart of the relative volume distribution in a Danfoss 3 kW inverter, FC 302. The pie chart does not include external harmonic and sine wave filters.

2% of the internal volume. The small dimensions of the power module of 12x5x2 cm results in a minor volume contribution, meaning decreasing the volume of the power module will produce a low relative impact on the overall power density of the converter. If the goal is to improve power density of the converter as a system, focus should not only be drawn towards increasing power density of the power module, but be expanded to its effect on external components as common and differential mode filters, DC-link and cooling. The reason for not considering chassis and control to be subjects for improvement is by the visual inspection performed during disassembly. Air accounts for 17% of the internal volume and based on the pie chart it present itself as a candidate for significant volume reduction. In practise however the air represented in the chart accounts for spacing between printed circuit boards (PCB) and chassis, air between components and air for electrical insulation. The photograph in figure 2.3 displays the air gab required between the chassis and the PCB due to varying heights of PCB mounted components.

The air between components, PCB and chassis are difficult to utilize, since the design already utilizes the space around PCBs and physical large components as filters and electrolytic capacitors. A large fraction of the control volume is contributed by the control card and its interface with display. The control is compact and consists of DSPs and small SMD components. The volume occupied for control could be minimized with the effect of reducing the external user interface. The user interface is assumed to be a fundamental requirement from the costumer and is therefore not treated as a possibility for volume improvements. The chassis serves as a heatsink and structural support for the converter. The design of the chassis is build around the components, making it a volume efficient design. The compactness of the converter chassis is also supported by the locations of the free air presented earlier. For the Danfoss converter unit a harmonic filter [12] and a sine wave filter [13] are included as a part of the converter system. The selection of additional components are provided

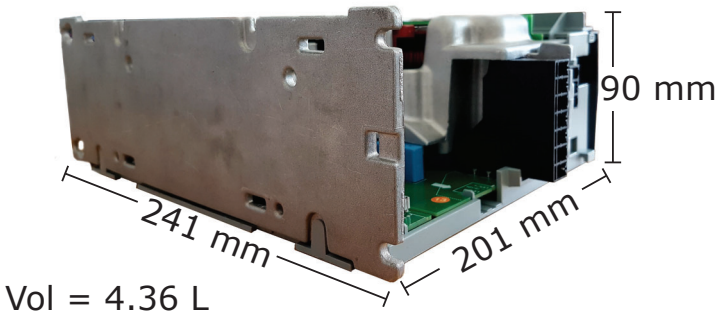

Figure 2.3: Disassembled Danfoss converter

by a system manager at Danfoss Drives.

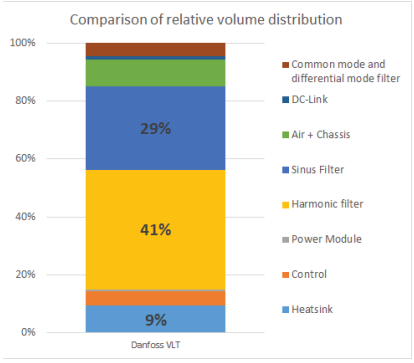

Figure 2.4: Relative volume distribution for the converters disassembled with selected numbers presented

Based on the disassembly of a state of the art variable frequency drive it is concluded that the power electronic packaging itself can not significantly reduce the volumetric size of the converter. The packing of semiconductors should therefore be chosen based on decreasing thermal impedance and the parasitic parameters to enable low loss operation of the semiconductor device. An example could be the need for low stray inductance for fast switching devices such as SiC MOSFETs and GaN transistors [14]-[15]. The focus points of the volume minimization for a Danfoss drive in respect to power electronics should therefore be on reducing power dissipation and the size of common and differential mode filters. By removing the requirement for harmonic and sine wave filters, a volume reduction by $\frac{2}{3}$ can be obtained. The switching frequency and the output voltage levels of the topology are therefore key factors in reducing the size of the passive filter components which today are a necessity for producing sinusoidal currents and voltages, at the input and output terminals.

With the major components in a converter identified, the next step is to narrow the

focus of which AC converter topology enables a high power density and efficiency with the new wide bandgap devices. The question of whether a hard switched or soft switched topology should be used, will therefore be addressed in the following section.

2.2 Soft or hard switching

Based on the experience gained from one of the finalists in the Google little box challenge a comparison study utilizing $\eta\rho$-Pareto optimization has been published [8]. The aim of the Google little box challenges was to build the world smallest single phase 2 kW converter, making their conclusion relevant when considering a 7.5 kW three phase inverter. One method of reducing the conduction losses and the output ripple current is to use an interleaved converter. Interleaving of a converter is obtained by parallel connecting multiple legs with individual inductors per phase. A principle schematic of interleaving a half bridge converter is shown in figure 2.5.

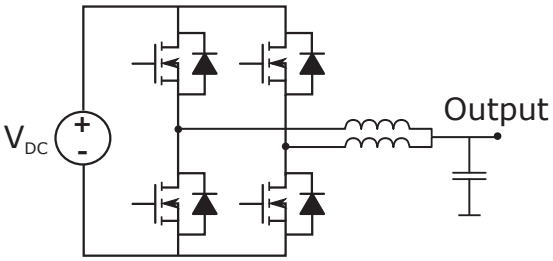

Figure 2.5: Circuit schematic of a interleaved single phase half bridge converter.

Their conclusion regarding interleaving is that it increases the efficiency (η) but requires twice the number of semiconductor devices and inductors yielding a lower converter power density (ρ), compared to what is obtainable without. Soft switching and hard switching is compared by power density for a zero voltage switching (ZVS) triangular current modulation (TCM) and a hard switched PWM modulation. The TCM obtains a higher efficiency but a lower power density. The cause of the lower power density is the need for zero current detection circuit, high current ripple across inductor and large RMS current compared to PWM modulation, resulting in a larger inductor and higher conduction losses. The benefit of decreased switching losses is therefore cancelled by the increase of losses in passive components. The results of their comparison is graphically represented in Figure 2.6

The converter comparison was performed on a single phase inverter. The topology utilized for obtaining the highest power density based on their research is a non-interleaved hard switched topology. Utilizing a hard switching PWM modulation introduces larger dV/dt during switching transients compared to soft switching. The high dV/dt are therefore crucial to address to maintain reliable operation and fulfilment of grid codes [16],[17].

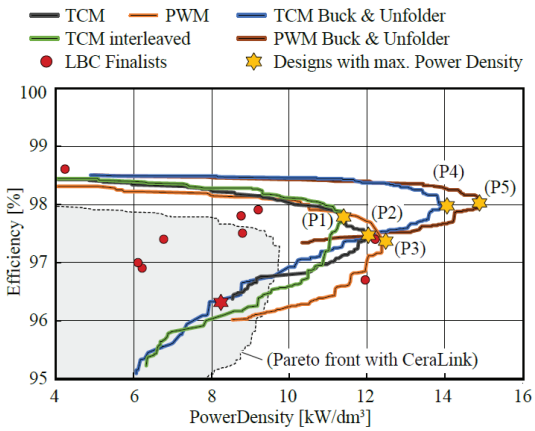

Figure 2.6: Results of calculated comparison study between TCM and PWM modulation schemes with and without interleaving [8]

2.3 Findings and limitations

Based on the information gathered from the previous sections, the focus for optimizing a converter, for high efficiency and high power density, can be defined. The focus and limitations for a high efficient and high power density converter will be:

- Hard switches topology
- non-interleaved converter
- Power module design should focus on minimizing power dissipation and thermal impedance
- Reduction of filter volume based on increasing switching frequency and/or topology
- Heatsink size should be reduced by selecting fitting semiconductor devices and switching frequency
- The optimum power density solution will be a compromise between heatsink and filter volume

Based on the key points stated above, an algorithm is developed to handle all the design variables. An algorithm is needed due to the vast solution space present, and to provide an enlightened selection of design parameters and components.

CHAPTER 3

Selection of topology and design parameters

This chapter present an in depth explanation of the Pareto optimization algorithm used to select the converter topology, components and design parameters. The structure of the algorithm, equations and assumption are presented and discussed.

The paper associated with this chapter (paper A) presents the main structure and working principle of the algorithm, with a special focus on the relationship between switching frequency and the power density, efficiency and cost.

- Paper A: Cost, Efficiency and Power Density Pareto Investigation of Three Phase Inverters.

In the result section of this chapter, a more detailed comparison of the different topologies are performed. The comparison is performed at an optimum switching frequency, quantifying the size of the major components for all topologies.

3.1 Introduction

As a case study a Danfoss 7.5kW VLT is used as a reference design for optimization. The focus of optimization will be on the DC/AC inverter stage. The inverter stage includes DC-link, heatsink, power module, gate driver and output filter. Due to the vast amount of combinations of filter designs, semiconductors, topologies and switching frequencies, selecting an optimum design becomes a challenging task [18]. An algorithm is therefore developed, evaluating the optimization objectives for thousands of designs, allowing for an educated guess on the specifications for the optimum converter. For the optimization algorithm different hard switches topologies are selected for investigation. The topologies includes a two level half-bridge, three level T-type and active neutral point clamped (ANPC), and a four level Pi-type converter. The schematics of the topologies are shown in figure 3.1.

Several advantages and disadvantages are present for each topology, making the selection of the optimum topology a challenging task. One of the major advantages utilizing a two-level converter is the small required DC-link capacitance. If the two level converter is supplying a three phase balanced load, the average output power during a switching period will be constant. The energy supplied from the DC link is as a consequence zero during one switching period. Zero capacitor current during a fundamental switching cycle are not guaranteed for multilevel converters without advanced control [19]. Multilevel converters without advanced control will experience low frequency DC-link power ripple with three times the fundamental frequency of the input

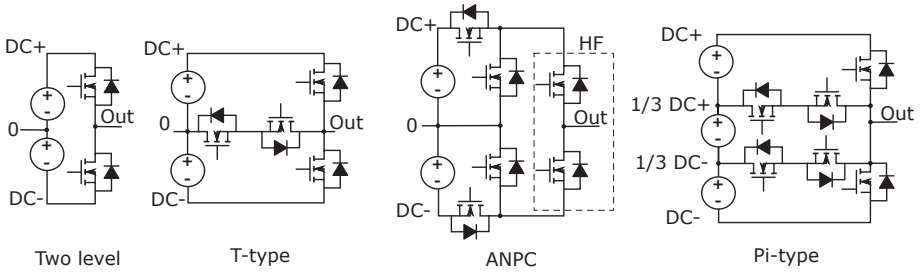

Figure 3.1: Converter topologies implemented in the Pareto optimization algorithm.

and output voltages. The low frequency power ripple results in larger requirement of DC-link capacitance. An advantage of utilizing a multilevel topology is the increase in output voltage levels which reduces the filter volume and power dissipation. General for the two level, T-type and Pi-type is that the switching and conduction losses are distributed between all the dies, which is not the case for the ANPC. The high frequency (HF) leg conducts the full current and is switched with a high frequency, resulting in the HF leg being responsible for the dominant part of the semiconductor losses. The low frequency (LF) switches are switched dependent on the fundamental output cycle, resulting in the main loss contribution from the low frequency switches being conductive.

Each topology will, as a consequence, have an optimum semiconductor combination, output filter, DC-link, heatsink and switching frequency depending on the optimization objectives. An objective comparison and selection of topology is therefore only accomplished by evaluating a large solution space of converter designs and comparing them by the prioritized optimization objectives. In this optimization algorithm the objectives are power density, efficiency and cost where power density and efficiency are favourable compared to system cost.

3.2 Optimization Algorithm

A $\eta\rho$\$-Pareto optimization is selected for the algorithm. As introduced in section 2.2 a front of possible design candidates are created based on the algorithm, allowing for the selection of the optimum design candidate. An optimum design candidate is defined as a design where the increase of one optimization objective results in a decrease of another. The calculation of losses, volumes and cost are based on analytical equations, allowing for fast computation. This allows for a full sweep of design variables as switching frequency and component libraries without having an unacceptable execution time. The overview of the optimization algorithm and the interconnection between the major components are shown in figure 3.2 for an inverter with output filter.

As indicated by figure 3.2 the input parameters are DC-link voltage, output power and junction temperature. The input parameter being swept is the switching frequency

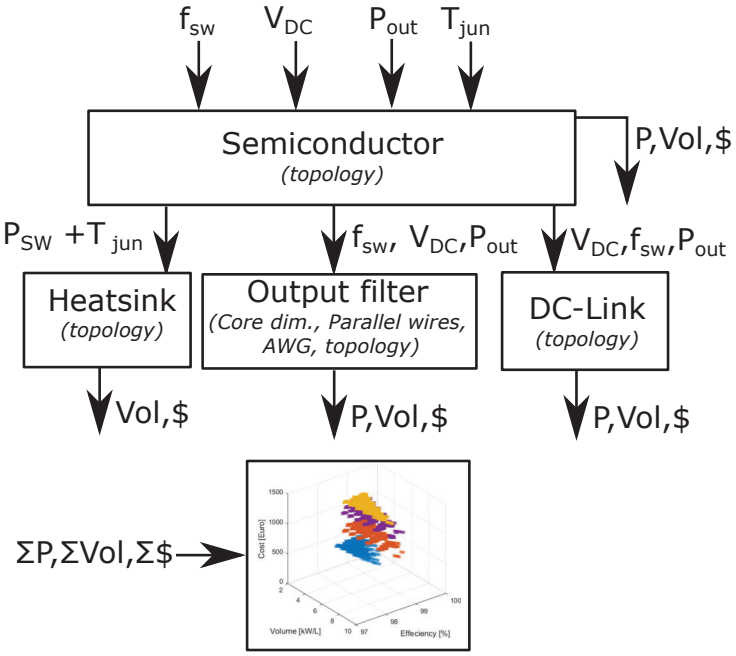

Figure 3.2: Flowchart of the Pareto optimization algorithm.

and topology. In the functions for each major components, the feasibility of the solution is evaluated. If the solution is not feasible it is removed from the solution space. An example could be the power dissipation of the semiconductor requiring a negative thermal impedance of the heatsink. The request of a negative thermal impedance is an indication of a power dissipation and a thermal impedance of the power module violating the maximum junction temperature. The design candidate is therefore removed due to it being an infeasible solution. In the following section a brief description of the models and assumptions for calculating volume, power dissipation and cost are presented for the major components.

3.2.1 Semiconductor

The losses associated with the semiconductor is separated into two groups: conduction losses and switching losses. The conduction losses is dependent on the current and a temperature dependent on-state resistance. The switching losses can be calculated using different methods as for example the switching loss curves given in the datasheet or analytical equations based on threshold voltage and time constants of the devices. However all these methods requires knowledge of the gate driver circuit, which heavily depends on the specific semiconductor devices, topology, power module and gate driver layout realised. It is therefore assumed that the switching losses are dominated by the contribution of the device output capacitance. The assumption is selected based

on published experience with GaN transistors [20]. It is assummed that the converter only performs hard switching, the soft switching occurring under certain operation points as a consequence of deadtime, load current and output capacitance is therefore not considered.

Conduction losses

The on-state resistance is implemented as a function of temperature by linear interpolation. The linear interpolation is presented in (3.1)

$$R_{ds}(T_j) = R_{ds(on)}(T_1) + \frac{R_{ds(on)}(T_2) - R_{ds(on)}(T_1)}{T_2 - T_1} \cdot (T_1 - T_j) \tag{3.1}$$

Temperature values T_1 and T_2 are the on-state resistance specified in the datasheet for two different temperatures, typically 25°C to 150°C. The junction temperature inserted into equation (3.1) is an input parameter initially specified in the algorithm for sizing the required volume for a heatsink.

Capacitive switching losses

The capacitive contribution of the switching are a sum of losses related to capacitors. Assuming the transistor to be modelled as a switched resistive element allows considering the circuit as a resistive charging of a capacitor. Resistive charging of a constant capacitance is performed with a 50 % efficiency ($\eta_{charging} = 50\%$) regardless of the resistance value [21]. Assuming the capacitances to be constant yields the conclusion that all capacitive loads connected to a transistor regardless of it being a non-ideel inductor or a semiconductor will contribute to the switching losses with the capacitive energy stored. An example of the switching transition for a T-type converter is presented in figure 3.3 with a DC-link voltage of 600 V. The circuit diagram will be used to carry out a calculation example of the capacitive losses, as a documentation of the procedure on which the future results presented will rely on.

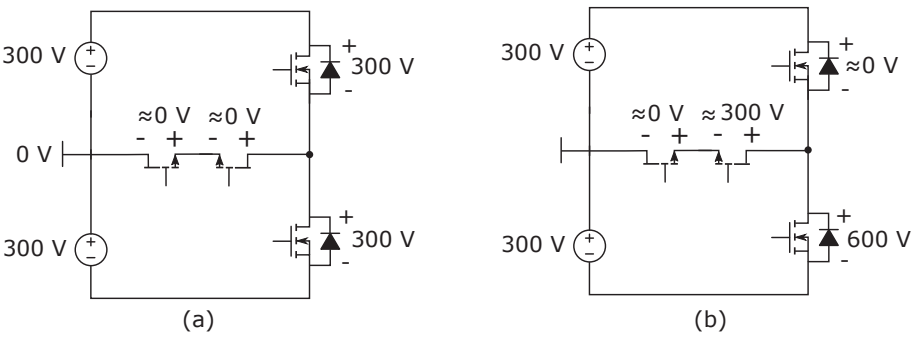

Figure 3.3: Example of differential voltages across devices during a switching transition.

The switching transition investigated in figure 3.3 (a) is with the middle leg conducting transitioning to figure 3.3 (b) with the top switch conducting. The top transistor will discharge the energy stored in its output capacitance through its channel and charge the externally connected transistors from 0 V to 300 V in the middle leg and 300 V to 600 V for the lower transistor. The contributions to the energy dissipated in the top switch during a turn on transient can be summarised by the three integrals given in (3.2) - (3.3). The middle leg consist of a serialised connection of two GaN transistors, presenting the increased complexity when considering a converter with different transistors implemented.

$$E_{oss(dis)} = \int_{300V}^{0V} C_{SiC-oss}(V) \cdot V \quad dV \tag{3.2}$$

$$E_{oss(charge)} = \int_{0V}^{300V} C_{GaN-oss}(V) \cdot V \quad dV + \int_{300V}^{600V} C_{SiC-oss}(V) \cdot V \quad dV \tag{3.3}$$

By performing the integration and including the two switching transitions per switching cycle, an equation for the switching losses can be derived as shown in 3.4.

$$P_{sw-cap} = 2 \cdot \sum (E_{oss-dis} + E_{oss-charge}) \cdot f_{sw} \tag{3.4}$$

The sum of switching losses and conduction losses are used as an input for the sizing of the heatsink.

Semiconductor library

The semiconductor library of the pareto scripts includes transistor of different materials from different manufacturers. The library contains GaN transistors from GaN systems, SiC MOSFET from Wolfspeed and ROHM, and Si MOSFETs with low on-state resistance for the ANPC. The device ratings are ranging from 650V to 1.2 kV, with a on-state resistance variation from 22mΩ to 120mΩ. An on-state resistance of 120mΩ is the limiting value, for the rated current.

3.2.2 Heatsink

Calculating the size of a heat sink is a complicated task, since accurate results in terms of thermal impedance requires solving the heat flow in 3D. An equation is defined to simplify the calculation. The equation is shown in equation (3.5) and assumes the thermal impedance to be inversely proportional to the volume of a heat sink.

$$K_{heat\ sink} = R_{th} \cdot Vol_{heatsink} \tag{3.5}$$

The heat sink constant can then be determined based on a datasheet of a heat sink. Doubling the volume of the heat sink will as a consequence half the thermal

impedance. The heat sink constant is calculated based on cooling with forced convection. The heat sink constant is given in (3.6) for a Coldcube heatsink [22].

$$K_{heat\,sink} = 0.12\frac{K}{W} \cdot 7.5cm \cdot 8.2cm \cdot 10.0cm = 73.8\frac{K \cdot cm^3}{W} \tag{3.6}$$

The ambient and the maximum allowed temperature for exposed components is specified in (3.7)

$$T_{amb} = 45°C \quad , \quad T_{max} = 70°C \quad , \quad \Delta T = 25°C \tag{3.7}$$

The required thermal impedance is calculated using equation (3.8).

$$R_{th} = \frac{\Delta T}{\sum P_{loss}} - \frac{R_{thermal\,compound} + R_{die-baseplate}}{n_{transistors}} \tag{3.8}$$

The thermal impedance can then be inserted into equation (3.6), solving for the heat sink volume. This method will be used for calculating the heat sink volume contribution.

3.2.3 Output filter

A typical two-level inverter as used in the Danfoss converter is shown in figure 3.4 with an L-C filter. An L-C filter is proposed for AC drives to suppress common mode

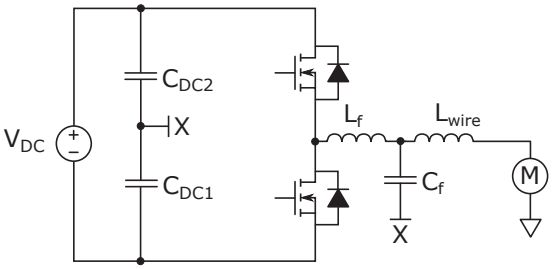

Figure 3.4: Two level inverter with output filter

(CM) and differential mode (DM) dv/dt [23], [24]. CM voltages introduces high frequency leakage currents through the bearings of the AC machine, reducing the motor reliability. The DM voltages can produce over voltages at the motor terminals if long cables are used. The terminal over voltage is twice the output voltage magnitude of the converter, increasing stress on insulation [25]. The output filter for all converter topologies will be based on the recommended L-C filter with the capacitor connected to the mid point of the DC-link.

Inductor

The calculation method for quantifying the volume and power dissipation of the inductor is based on the geometric size of the core, diameter of the windings, copper

losses, switching and fundamental frequency core losses. The core dimensions are obtained from manufactures [26] and used as inputs for the model. In figure 3.5 the notation of the core dimensions are specified.

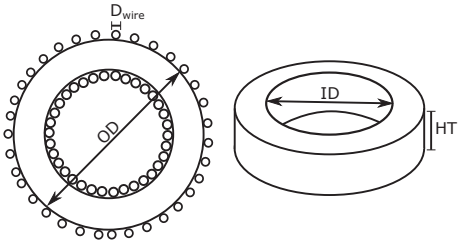

Figure 3.5: Specification of core dimension used for calculating the volume of the inductor.

The MATLAB script utilizes the core dimension to calculate the physical limit of the number of windings using equation (3.9).

$$N_{\text{physical}} = \frac{ID}{n_{parallel} \cdot D_{wire}} \tag{3.9}$$

A constraint is set by the potential core saturation, the maximum number of windings before saturation is therefore calculated. The lowest integer value of windings is used for further calculations in the script. The number of windings is used to calculate the inductance value, allowing the algorithm to select suitable inductors for each topology and switching frequency [27]. The volume of the inductor is calculated using equation (3.10)

$$\text{Vol}_L = \frac{\pi \cdot (OD + 2 \cdot D_{wire})^2}{4} \cdot (HT + 2 \cdot D_{wire}) \tag{3.10}$$

With the inductance associated with a certain volume, the next step is to calculate the core losses of the inductor. To calculate the losses, the variation in magnetic field strength is initially calculated by (3.11).

$$H_{ripple-max/min} = \frac{N \cdot (I_{RMS} \pm \frac{I_{ripple}}{2})}{l_e} \tag{3.11}$$

The magnetic field strength can then by used to determine the magnetic flux density ripple by an empirical equation as (3.12) [28].

$$B_{ripple-max} = \left(\frac{a + b \cdot H_{ripple-max} + c \cdot (H_{ripple-max})^2}{1 + d \cdot H_{ripple-max} + e \cdot (H_{ripple-max})^2} \right)^x \tag{3.12}$$

From equation (3.12), the magnetic flux density ripple is obtained for a specific DC current bias. The core losses caused by the current ripple are calculated based on

the RMS current of the sine wave. The equation for the magnetic flux density ripple is presented in (3.13)

$$B_{pk} = \frac{B_{AC-max} - B_{AC-min}}{2} \tag{3.13}$$

The power dissipation per volume core is then calculated based on the flux ripple caused by the fundamental output frequency and the switching frequency. The empirical equation is presented in (3.14), [29].

$$PL = a \cdot B_{pk}^{b} \cdot f^{c} \quad [\mathrm{mW/cm^3}] \tag{3.14}$$

Based on (3.14) and the volume of the core, the hysteresis losses can be calculated for each inductor design. The copper loss is separated into the DC and AC component where only the calculation method of the AC component will be presented. The calculation of the AC conduction loss is based on the skin depth and the length of the wire. The length of the wire is calculated using equation (3.15)

$$l_{wire} = N \cdot 2 \cdot (HT + OD - ID + D_{wire}) \tag{3.15}$$

where ID, OD and HT describes the dimension of the core, D_{wire} being the wire diameter and N being the number of windings. The skin depth is given by equation (3.16).

$$d_{cu} = \sqrt{\frac{\rho_{cu}}{\pi \cdot f_{sw} \cdot \mu_0 \cdot \mu_r}} \tag{3.16}$$

With the skin depth and wire length determined, the ac resistance of the wire can then be determined by (3.17).

$$R_{AC} = \frac{l_{wire} \cdot \rho_{cu}}{\frac{\pi}{4}(D_{wire}^2 - (D_{wire} - 2 \cdot d_{cu})^2) \cdot n_{parallel}} \tag{3.17}$$

Combining the core, DC and AC copper losses the total power loss of the inductor can be calculated. A constraints for the possible inductor solutions is set by a maximum temperature of 70°C. The manufacture of the Kool Mu cores (MAGNETICS) provides an empirical equation for temperature rise of the inductor. The equation is given in (3.18).

$$\delta T_{core} = \left(\frac{P_{loss} \cdot 10^3}{A_{surface} \cdot 10^4} \right)^{0.833} \tag{3.18}$$

The temperature constraints is used in the final script to reduce the solution space, by removing the inductors which would exceed the maximum allowed temperature.

Capacitor

The capacitance value of the L-C filter is selected to obtain a specific filter cut off frequency. The cut off frequency is selected to be the logarithmic middle of the switching frequency and the highest fundamental output frequency. Utilizing this as a design criteria, the cut off frequency of the filter can be determined by (3.19).

$$\omega_{\mathrm{LC}} = 2 \cdot \pi \cdot 10^{\frac{\log(f_{\mathrm{fund}})+\log(f_{\mathrm{sw}})}{2}} \tag{3.19}$$

With the cut off frequency and inductance known the capacitance value can be determined by (3.20).

$$C_{\mathrm{f}} = \frac{1}{L_{\mathrm{f}} \cdot {\omega_{\mathrm{LC}}}^2} \tag{3.20}$$

With a fundamental frequency of 590 Hz, switching frequency of 100 kHz and an inductance value of 216.5 μH.

$$C_f = \frac{1}{216.5\mu H \cdot (2 \cdot \pi \cdot 7.7kHz)^2} = 2\mu F \tag{3.21}$$

The low value of capacitance required for the filter allows for the usage of multi layer ceramic capacitors (MLCC) or a small film capacitor. The volume of the capacitor is therefore small compared to the volume contribution of the inductor.

3.2.4 Cost

The cost is an important parameter, which is expected to increase with the number of semiconductor devices. To evaluate the cost dependency of efficiency, power density and topology, prices are added for the major components.

Semiconductors

The price of the semiconductors are included as the price for the devices in a discrete package. The prices are found on Mouser Electronics, an electronic components distributor. The prices of components are found at one distributor, making them comparable in relativemagnitude.

Gate driver

The gate driver cost is calculated based on number and type of components utilized. The script distinguishes between a single and dual gate drivers. The dual gate drivers are used for the middle leg switches in multilevel topologies. The components allocated for the single and dual gate drivers are listed in (3.22) and (3.23) respectively.

$$\mathrm{cost}_{\text{GD-single}} = \mathrm{price}_{\mathrm{GD}} + \mathrm{price}_{\mathrm{DC/DC}} + 9 \cdot \mathrm{price}_{\mathrm{cap}} \tag{3.22}$$

$$\mathrm{cost}_{\text{GD-dual}} = 2 \cdot \mathrm{price}_{\mathrm{GD}} + \mathrm{price}_{\mathrm{DC/DC}} + 13 \cdot \mathrm{price}_{\mathrm{cap}} \tag{3.23}$$

The components significantly contributing to the price of the gate drivers are the gate driver IC and the isolated DC/DC power supply. The gate driver circuit accounts for a significant cost contribution of the complete converter system [30].

Heatsink

The cost of a heatsink is calculated based on the volume. The heatsink is assumed to be made from a solid piece of aluminium. The volume is therefore used to calculated the weight of the solid aluminium piece being used for the heatsink. The price for a kilo gram of aluminimum is then used to obtain the price of a heatsink. The equation is presented in (3.24)

$$\text{Cost}_{\text{heatsink}} = \text{Vol}_{\text{heatsink}} \cdot \rho_{alu} \cdot \text{price/kg} \tag{3.24}$$

The aluminium price is very low compared to the semiconductor devices and gate drivers, meaning the cost contribution is insignificant when comparing to the final cost of the inverter.

Inductor

The core dimensions and volumes are known in the script, due to it being a necessary part in the inductor design procedure. The inductor cost is calculated with a similar method as the heatsink. The price of the inductor is as a consequence proportional to the core volume. The equation is presented in equation (3.25).

$$\text{Cost}_{\text{L}} = \text{Vol}_{\text{L}} \cdot \frac{\text{price}}{\text{m}^3} \tag{3.25}$$

3.3 Results

The purpose of this section is to present the combined results of the modelling shown in section 3.2. The combination of models will provide a full system evaluation of power density, efficiency and cost. The component library used in the algorithm consist of commercially available products. Each point in the Pareto optimization is therefore a full system evaluation, with an attached bill of materials. The complete solution space of thousand of converter combinations provides an objective comparison between different topologies, design parameters and components on a system level.

3.3.1 Cost, Efficiency and Power Density

The three dimensional Pareto plot can be seen in figure 3.6 sweeping a frequency range from 25 kHz to 150 kHz with an output RMS current of 16 A. The efficiency and power density front of the results is shown in figure 3.7.

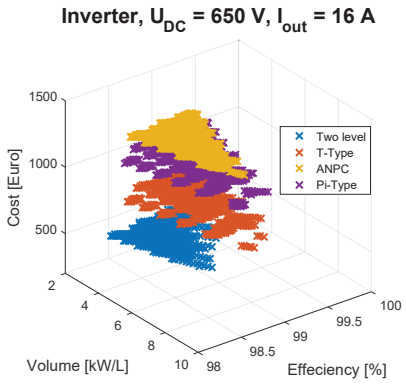

Figure 3.6: Three dimensional Pareto plot of an inverter including cost, efficiency and power density.

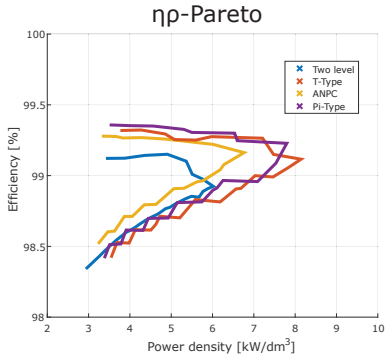

Figure 3.7: Extracted efficiency and power density Pareto front.

When evaluating figure 3.6, relative small improvements in power density and efficiency are achieved compared to the conventional two level topology. Moving to a multilevel topology, requiring additional semiconductor increases power density and efficiency but also heavily increase the price of the converter. The converter price being heavily dependent on the semiconductor count are expected as the price of SiC MOSFET, GaN transistors, DC/DC converters and gate drivers are high compared to the price of aluminium and filter cores. The benefit of performing an objective selection of components and design parameters based on a system evaluate is clear, when evaluating on the spread of possible solutions for each topology. The correct selection of semiconductors, switching frequency and inductor design are just as important as the selection of the optimum topology.

The two level converter achieves the lowest efficiency due to the large switching and hysteresis losses, which limits the obtainable switching frequency. The low efficiency therefore results in a low power density due to the large inductor and heat sink volume required.

Comparing the power densities and efficiencies of all topologies, the most significant improvement is observed when changing from a two level topology to a three level topology. Most noticeably is the benefit when selecting a T-type topology. The T-type topology reduces switching losses and decreases the required inductance of the filter [31]. The semiconductor losses are distributed on all four dies during a fundamental period, reducing the size of the heatsink. The low switching losses and conduction losses enables a very high efficiency. Of all topologies the ANPC has the lowest switching losses, due to the reduced required blocking voltage enabling the use of GaN transistors. The ANPC is therefore suitable for high switching frequencies. The disadvantage of the GaN transistor is the high conduction losses at higher temperatures. The GaN on-state resistance increases by a factor of 2.5, with a temperature increase from 25°C to 150°C. In combination with the low resistance Si MOSFETs in the topology, the increased conduction loss outweighs the benefit of low switching

losses for the specific specifications investigated. Figure 3.7 shows nearly equal efficiency being achieved by the four level Pi-type and the three level T-type converter. The reason being, adding another output voltage level will reduce the switching and filter losses, but increase the conduction losses.

An in depth view of the volume distributions for each topology is presented in figure 3.8 for a switching frequency of 70 kHz. A switching frequency of 70 kHz is selected, due to the high power density and efficiency achieved for all topologies.

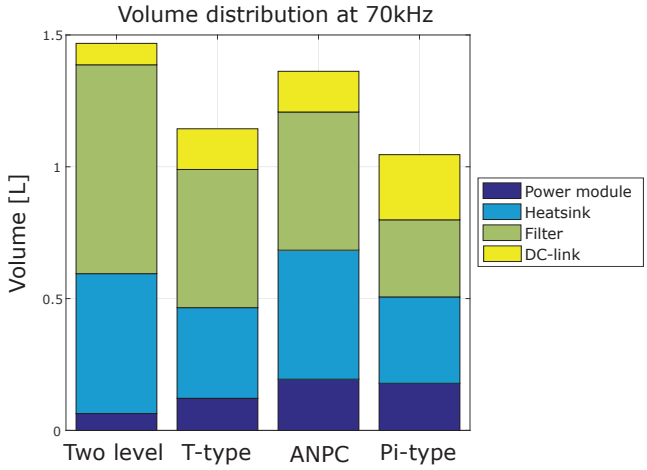

Figure 3.8: Volume distribution of major components

The volume of the major components in figure 3.8, shows a significant volume reduction is obtained by changing from a two level topology to a T-type topology. The volume reduction is obtained by the decrease of required output filter and heatsink volume. The ANPC achieves a lower power density than the T-type, due to the power loss being concentrated on two transistors, and the fact that the topology needs six switches with gate drivers. The Pi-type topology achieves the highest power density. The increase in power density from a T-type to a Pi-type is however small compared to the improvement obtained from a two level to a T-type. The added cost from additional switches and gate driver circuitry needed for ANPC and Pi-Type converter can not be justified in respect to converter price and performance gain.

3.3.2 Selection of topology

Based on the results from the Pareto algorithm an objective comparison between the conventional two level converter and multilevel alternatives are performed. All multilevel topologies investigated in the Pareto algorithm achieves higher power densities and efficiencies compared to the two level converter.

Compared to the conventional two level converter, the selection of a T-type topology can be justified by its increase in power density and efficiency, with the penalty of a significant cost increase. Choosing a topology with additional transistor or out-

Table 3.1: Main values and components for the T-type converter at 70 kHz

Parameter	**Value**
Power (P_{out})	7.5 kW
Current (I_{RMS})	16 A
switching frequency (f_{sw})	70 kHz
SiC MOSFET	25mΩ
Inductor (Kool Mu)	380uH
Power density	7kW/dm^3
Efficiency	99.2 %
Cost	700 $

put voltage levels compared to the T-type can not be justified, due to the insignificant performance improvements with a significant increase in cost, control complexity and reduced manufacturability. The Pareto algorithm present the two level and the T-type converter as ideal design candidates. The compromise is between the cheaper two level topology or the more expensive T-type converter, which achieves a higher power density and efficiency.

The goal of the thesis is to build a converter with a high power density and efficiency, resulting in the selection of a T-type converter. The bill of material is extracted for the solutions at a switching frequency of 70 kHz. A switching frequency of 70 kHz is selected due to the high power density and efficiency achieved simultaneously. Increasing the switching frequency above 70 kHz, will increase the volume of the heatsink, which is not justified by the reduction of filter volume. The losses of the converter at 70 kHz is dominated by the semiconductor losses, meaning increasing the switching frequency further will only decrease the overall system efficiency. The design parameters and key components of the T-type converter at 70kHz is presented in table 3.1.

CHAPTER 4

Validation of digital approach

The focus of this chapter is on the methodology related to the design process, the digital simulation with parasitics and the validation of it.

The paper associated with this chapter (Paper B) has a main focus on the experimental validation of the parasitic values and its impact on a converter operating at high voltage with high dV/dt.

- Paper B: Common Mode Current Mitigation for Medium Voltage Half Bridge SiC Modules

4.1 Introduction

With fast switching wide bandgap devices, higher dv/dt and di/dt introduces challenges in regards to over voltages, false turn on, EMI, performing measurements and control fidelity [32], [33]. A model for evaluating the performance of a converter layout before manufacturing is much needed, as new challenges appears and the means of validation are reduced. The model is particularly useful in the design phase to quantify the advantages and disadvantages of the design choices. Enabling digital iterations of optimization, without the need of a physical prototype. Avoiding a physical prototype in the design iteration reduces cost and saves time spend on experimental measurements. A flowchart describing how the digital model can be used in the design phase is presented in figure 4.1. The collection of simulation models are referred to as the digital twin.

Before using the digital twin for optimization, a validation of the method is needed. The modelling method is validated by developing a simulation model for a 10 kV SiC halfbridge converter and performing experimental measurements for validation. The converter is operated at 5kV and with a rated current of 10 A. The SiC MOSFET will therefore introduce large dv/dt and low di/dt [34]. Due to the high dv/dt the impact of capacitive coupling is important to address [35],[36]. The focus of modelling and validation will therefore be on the parasitic capacitance network created between the power module and the heatsink, as the capacitance contribution significantly effects both switching and EMI performance [37]. The parasitics values are extracted from the layout using Ansys Q3D Extractor. The parasitics are combined with models of semiconductors and passive components to establish an accurate digital twin.

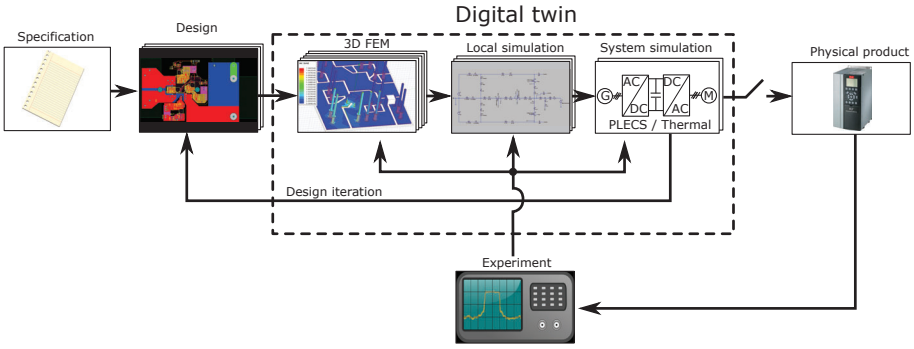

Figure 4.1: Flowchart of the digital design iterations using a digital twin

4.2 System modelling

The structure of a conventional power module introduce large capacitive couplings, due to its sandwich structure. The layers of a power module is presented in figure 4.2. Parasitic capacitive couplings are created between the copper planes separated by the isolating ceramic. The thickness of the ceramic is desired to be kept low for improving the thermal performance of the power module, with the side effect of increasing the capacitive coupling. The capacitance value depends on the surface area, thickness and permeability of the isolating layer, as indicated in equation (4.1).

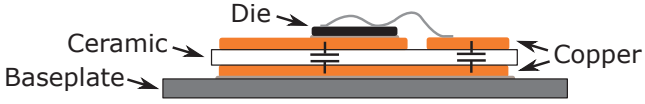

Figure 4.2: Structure of DBC

$$C = \frac{\varepsilon \cdot A}{d} \tag{4.1}$$

The capacitive network coupling a halfbridge power module and a heatsink is shown figure 4.3. In the schematic, parasitics couplings from measurement equipment, fans and grounding impedance are included. In a halfbridge the copper plane connected to the output terminal experience a high dv/dt, which in combination with the surface area required for dies and terminals results in a large capacitive current. Table 4.1 presents the capacitive couplings from the power module which were extracted using ANSYS Q3D Extractor [38].

If the heatsink is allowed to be floating, the parasitic network will become a capacitive voltage divider. The voltage potential of the heatsink will depend on the ratio between $C_{\sigma-}$, $C_{\sigma+}$ and $C_{\sigma out}$. Allowing the heatsink to float will reduce the switching loss contribution of the parasitic capacitances and the magnitude of the capacitive current. One key concern with a floating heatsink is the safety of the personal. Since a

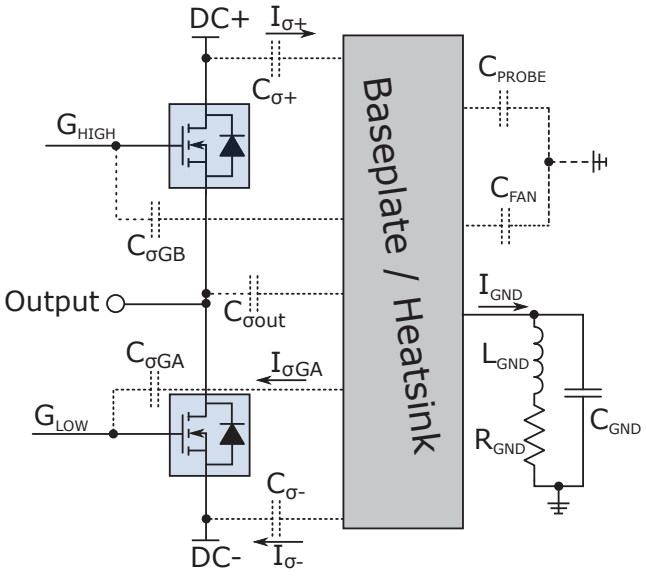

Figure 4.3: Parasitic network of a half bridge module coupled with baseplate.

floating heatsink might reach several kilovolts due to high DC-link voltages, dv/dt and coupling capacitances. Having a floating heatsink is therefore excluded as an option due to safety. A grounding impedance is therefore proposed to control the voltage of the heatsink. The grounding of the heatsink increases capacitive switching losses and capacitive current. The modelling of the heatsink impedance network, can be simplified analytically by paralleling the capacitive contributions. Due to the high switching speed the frequency response of kHz to MHz are of interest. DC voltage source and 50 Hz AC source can as a consequence be replaced with a short circuit. The capacitive couplings from $C_{\sigma+}$, C_{probe}, C_{fan}, $C_{\sigma GA}$ and $C_{\sigma-}$ can be summed together as shown in equation (4.2), the capacitive couplings $C_{\sigma out}$ and $C_{\sigma GB}$ experiencing the dV/dt of the output terminals are summed in equation (4.3) and the grounding impedance is given in equation (4.4)

$$\frac{1}{Z_2(s)} = \frac{(C_{\sigma+} + C_{\sigma-} + C_{\sigma\mathrm{GA}}) \cdot s}{R_{\mathrm{ESR}} \cdot (C_{\sigma+} + C_{\sigma-} + C_{\sigma\mathrm{GA}}) \cdot s + 1} \tag{4.2}$$

$$\frac{1}{Z_1(s)} = \frac{(C_{\sigma\mathrm{out}} + C_{\sigma\mathrm{GB}}) \cdot s}{R_{\mathrm{ESR}} \cdot (C_{\sigma\mathrm{out}} + C_{\sigma\mathrm{GB}}) \cdot s + 1} \tag{4.3}$$

$$Z_{\mathrm{GND}}(s) = \frac{\frac{1}{C_{\mathrm{GND}}} \cdot s + \frac{R_{\mathrm{GND}}}{L_{\mathrm{GND}} \cdot C_{\mathrm{GND}}}}{s^2 + \frac{R_{\mathrm{GND}}}{L_{\mathrm{GND}}} \cdot s + \frac{1}{L_{\mathrm{GND}} \cdot C_{\mathrm{GND}}}} \tag{4.4}$$

Based on equation 4.2 - 4.4 a small signal model of the voltage can be derived. The block diagram of the small signal model is shown in figure 4.4.

Table 4.1: Parasitic parameter values for heat sink modelling

Parameter	Value	Determination
$C_{\sigma+}$	100.5 pF	ANSYS Q3D
$C_{\sigma GB}$	21.6 pF	...
$C_{\sigma out}$	149 pF	...
$C_{\sigma GA}$	18.7 pF	...
$C_{\sigma-}$	45 pF	...
C_{PROBE}	8 pF	Impedance analyser
C_{FAN}	80 pF	...
R_{GND}	235 Ω	...
L_{GND}	25 μH	...
C_{GND}	50 pF	...

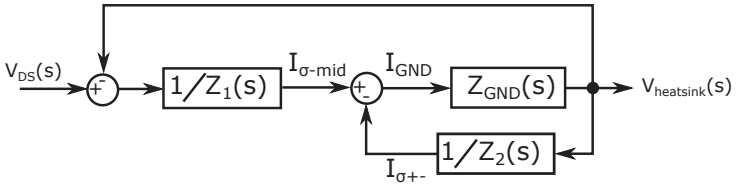

Figure 4.4: Block diagram of the impedance network related to grounding impedance of the heatsink, Z_{GND}.

If the model of the heatsink voltage and current is accurate compared to the measurements, it will be a validation of the understanding of the 10kV converter system and the parasitics extracted using finite element software. Deviations might provide useful informations about uncertainties of parasitic parameters and neglected contributions.

4.3 Experimental Setup

Th double pulse setup consists of a 10kV half bridge power module, protection board, interface card, DC-link and gate drivers. The obtainable DC-link voltage of the double pulse is limited by the 5 kV rating of the DC-link capacitors. The experimental setup is shown in figure 4.5.

4.3.1 Power module

The packaging of the 10 kV half bridge power module is performed at the Department of Energy Technology at Aalborg University. The power module used for the double pulse test is shown in figure 4.6. Holders for temperature measurements using optic

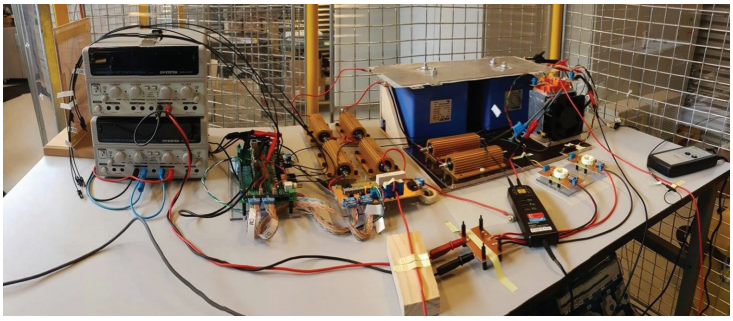

Figure 4.5: Picture of experimental setup

fibers are placed in the power module. Using optic fibers, the junction temperature of MOSFETs and diodes can be measured, without reducing the rated blocking voltage.

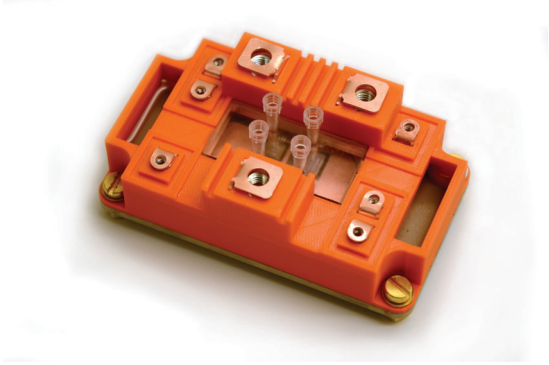

Figure 4.6: Picture of power module

During the manufacturing processes from DBC design to packaging, 3D models are generated for all components. 3D models of components facilitates the use of finite element software for parasitic extraction.

4.3.2 Gate driver design

When developing a gate driver circuit for wide bandgap devices, it is desired to utilize a minimum value of gate resistance. A minimum value of gate resistance will ensure low switching losses. The value of gate resistance is limited by over/under voltages and Miller induced false turn on [39], [40]. To effectively mitigate miller induced false turn on, a gate driver circuit utilizing an active Miller clamp is designed as shown in figure 4.7 and 4.8 [41]. The miller clamp provides a low impedance path for the Miller current, when the complementary switch is turned on [42]. The Miller clamp mitigates an undesired rise of the gate voltage, preventing false turn on.

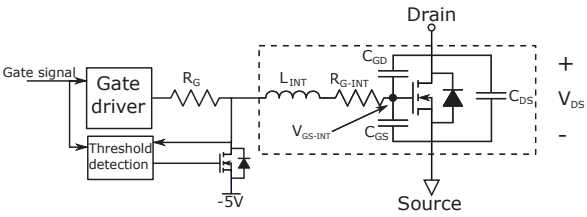

Figure 4.7: Gate driver schematic

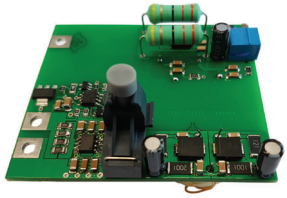

Figure 4.8: physical realization of gate driver

4.3.3 Results

In figure 4.9 a comparison between the measurement and simulation results at 5kV is presented. The dV/dt from the measured double pulse is used as an input for the simulation model. The dv/dt is used as an input, due to the unavailability of 10 kV MOSFETs models, at the time.

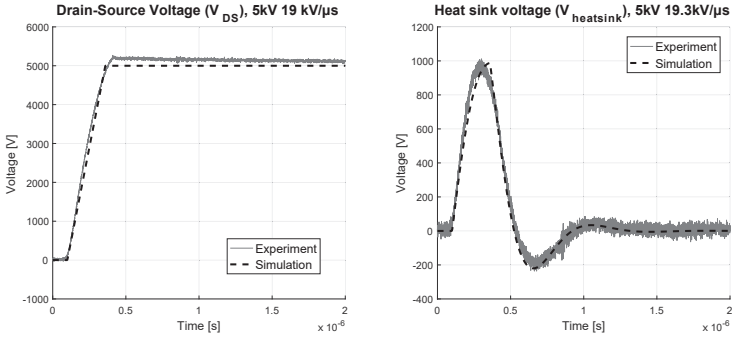

Figure 4.9: Comparison of simulation and measurement results at 5 kV

From figure 4.9 an excellent agreement between simulation and measurement can be identified. The good agreement between simulation model and experiment validates the impedance network and that magnitude of the capacitances extracted. The voltage magnitude, damping and time period heavily depends on the magnitude of the capacitances. The sensitivity is tested by removing the capacitance contribution from auxiliary equipment. In figure 4.10 the comparison between measured and simulation heatsink voltage with and without the auxiliary capacitance contribution are shown. The auxiliary equipment includes capacitance contribution from fan and probe, in total being a difference of 88 pF in capacitance.

By comparing the simulation results with and without auxiliary equipment a clear deviation in amplitude and ringing period can be identified. The damping remains unchanged, due to the ground impedance being unchanged. The sensitivity and good agreement between measurement and simulation demonstrates the validity of the dig-

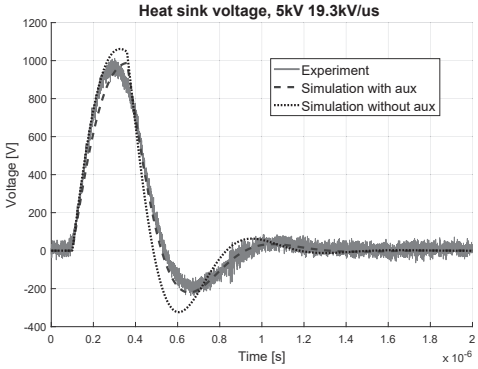

Figure 4.10: Comparison of simulation and measurement results at 5 kV

ital twin approach. The validated model would allow a designer to optimize the power module DBC digitally, and to evaluate the performance improvements gained. Improvements to the power module DBC layout was performed, reducing the output capacitive coupling by 50%. The impact of the improvements were equivalently validated using the double pulse setup.

4.4 Conclusion

To validate the digital prototyping using a digital twin, a 10 kV SiC half bridge converter was build. The purpose of the 10 kV was to experimentally validate the layout parasitics extracted using finite element software. Due to the high voltage and low current rating of the 10 kV SiC MOSFET dies, the focus were on the parasitic capacitances. By comparing the simulation with the experimental results, an excellent agreement was obtained. The good agreement increases the confidence in using finite element software to evaluate the performance of a design. Enabling the designer to perform design iterations using the digital twin model, avoiding expensive and time consuming design iterations driven by experiments.

CHAPTER 5

Building a single phase high density converter

This chapter presents the initial design process of a single phase T-type converter, including power module, power routing PCB and gate driver PCB. The focus is on quantifying the physical size of the different components, justifying the focus on minimizing the cost and size of the gate driver circuit using a bootstrap supply.

The paper associated with this chapter (paper C) provides a detailed mathematical approach for calculating the modulation index limit of a bootstrap circuit, together with a proposed bootstrap circuit for a T-type converter and its numerical validation.

- Paper C: Modulation limit of bootstrap power supply circuits: case study of a three level T-type converter

The performance results of the bootstrap circuit is presented at the end of this chapter, with a clarification of its limitations and the applicability in the prototype is discussed

5.1 Introduction

With the model methodlogy validated, the next step is to build the initial design layout of the 7.5 kW three phase inverter. For the inverter a T-type topology utilizing SiC MOSFETs is selected, based on a detailed Pareto optimization, presented in chapter 3. The schematic of the full three phase T-type converter is shown in figure 5.1.

The purpose of the initial design is to quantify the effect of parasitics, enabling a focused optimization of the layout. When referring to the converter layout, three components are considered. The components includes gate driver PCB, power routing PCB and power module. The layout of these components are of particular importance, due to their direct influence on the system efficiency and power density. When designing the layout of the power module and PCBs, a common constraint is the required clearance between different voltage potentials. The functionality of the clearance distance is to ensure electrical isolation. The required clearance distance depends on the pollution degree, isolation material and voltage difference for the given application. As a specific working environment is not specified, the generic standard on PCB design IPC2221A is used [43]. The standard is graphically illustrated in figure 5.2 at higher voltages.

Due to the configuration of a T-type, a blocking voltage potential of 400V from DC+ or DC- to MID is needed. A minimum distance between pins and copper planes

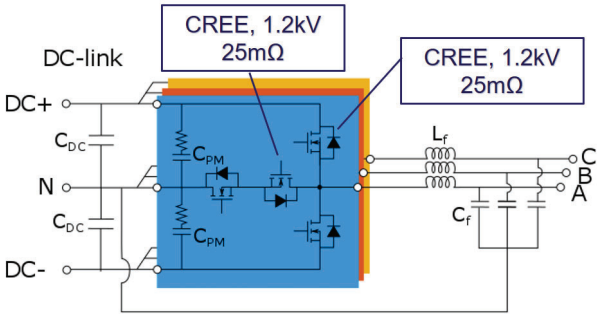

Figure 5.1: Graphical illustration of the semiconductor conductor dies selected

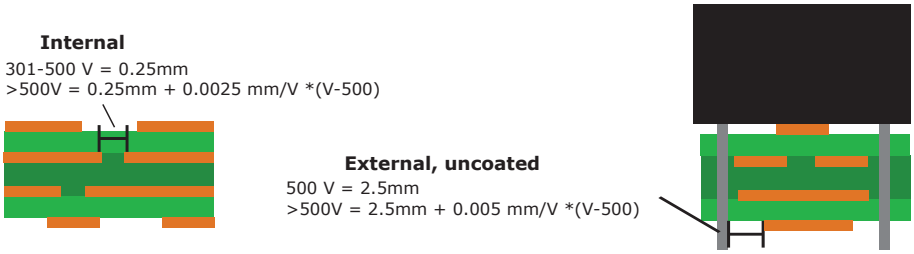

Figure 5.2: Graphic illustration of IPC2221A standard

of 2.5mm is therefore required, limiting the compactness of the layout. Inside the power module, Silicon gel provides electrical isolation. The power module terminals needs to fulfil the standard, as they are exposed outside the silicon gel. To quantify the area and volume required for the PCBs and power module, each part is designed in an appropriate software. The PCB layout is designed in Altium Designer and the power module is designed in SolidWorks.

5.2 T-Type Power module

The main functionalities of the power module is to ensure electrical connection from the gate driver and power routing PCB to the semiconductor dies and a low thermal impedance from the semiconductor dies to the heatsink. For the initial power module prototype an Easy 1B housing from Infinion is utilized. The Easy 1B is a small power module housing, with the dimensions 63mm (W) · 34mm (D) · 11.5mm (H). The DBC area is large enough to accommodate a single phase T-type converter, while complying with the IPC2221A standard. The Easy 1B housing is compatible with press fit terminals determining the connection to external PCBs. The power module housing with terminals can be seen in figure 5.3. An exploded view of the power module can be seen in figure 5.4 including bondwires, terminals, internal DC-link,

semiconductor dies DBC and housing.

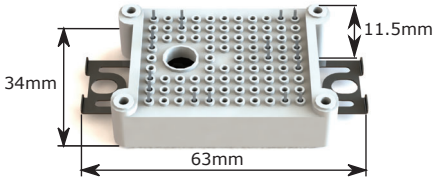

Figure 5.3: 3D rendered power module housing

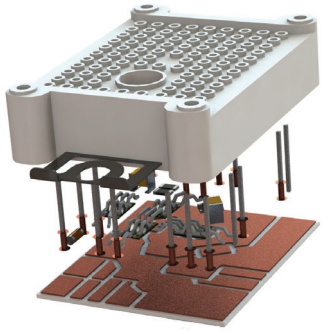

Figure 5.4: Three dimensional SolidWorks rendering of power module.

When utilizing the Easy 1B power module a total number of 18 pins are required. The large number of pins and the required external clearance introduces a layout limitation for the PCB design.

5.2.1 Selection of DBC material

The ceramic substrate of the DBC ensure an electrical isolation from the semiconductors to the heatsink. The insulating material between the semiconductors and the heatsink, increases the thermal impedance and thereby decrease the thermal performance of the cooling system. It is therefore important to select a suitable DBC material for the power modules. A comparison between the two DBC materails available at Aalborg University will be carried out, to determine the optimum selection of DBC material when using wide bandgap devices. The two DBC materials in stock are aluminium oxide (Al_2O_3) and aluminium nitride (AlN). The aluminium oxide has a lower cost compared to the aluminium nitride. The disadvantage of the aluminium oxide is a low thermal conductivity, compared to aluminium nitride. Therefore a price and performance comparison is needed to select the optimum material.

A DBC mastercard can be populated with 15 DBC patterns for Easy 1B housings. Using the more expensive aluminum nitride mastercard, the cost for per DBC is very low compared to the overall converter price. The DBC material should, as a consequence, be selected based on their thermal performance, to reach a higher power density.

The thermal conductivity is calculated using equation (5.1). Where A_{die} is the die surface area, f_i is the spreading factor, K_i is the thermal conductivity and l_i is the length.

$$R_{th} = \frac{1}{A_{die}} \cdot \sum \frac{l_i}{f_i \cdot K_i} \tag{5.1}$$

In table 5.1, the thermal conductivity and length of each layer is specified.

Table 5.1: Conductivity and layer thickness in a power module.

	Length	Thermal conductivity
Solder	50μm	63 $\frac{W}{m \cdot K}$
Copper	0.3mm	394 $\frac{W}{m \cdot K}$
DBC (Al_2O_3)	0.633mm	24 $\frac{W}{m \cdot K}$
DBC (AlN)	0.633mm	170 $\frac{W}{m \cdot K}$
Copper	0.3mm	394 $\frac{W}{m \cdot K}$
Thermal interface material (TIM)	100μm	0.58 - 8.5 $\frac{W}{m \cdot K}$

Based on equation (5.1) and the properties listed in table 5.1, the thermal conductivity of aluminum oxide and aluminum nitride DBC are calculated. The thermal impedances calculated are shown below, using a spreading factor of 1 and a thermal conductivity for TIM of 5 .

- R_{th-AlN} = 1 K/W
- $R_{th-Al_2O_3}$ = 1.87 K/W

Based on the thermal impedances calculated, a reduction above 45% can be obtained in thermal impedance, by utilizing aluminium nitride. The DBC used for the demonstrator is AlN, as a consequence of the estimated thermal impedance.

5.3 Gate driver

The gate driver is designed for the T-type with a special focus on minimizing the gate loop inductance, to minimize the voltage overshoot occurring across gate-source of the semiconductor [44]. To minimize the inductance contribution the gate driver IC, decoupling capacitors and resistor are placed near the gate-source terminals, minimizing the loop length. The isolated DC/DC supply and the digital isolator are placed beside the power module as shown in figure 5.5, due to the physical large dimensions of the DC/DC converter and the required clearance distance.

As can be seen from figure 5.5, the gate driver PCB occupies three times the surface area of the power module. The limiting factor for the compactness of the gate driver is the clearance requirement of 2.5mm and the size of isolated DC/DC converters. A more compact gate driver design could as a consequence be achieved by reducing the need of isolated DC/DC converters. One method of reducing the DC/DC converter count is utilizing a bootstrap voltage supply. A bootstrap supply uses resistors, diodes and capacitors instead of isolated DC/DC converters, making it, a volume and cost efficient solution [45],[46].

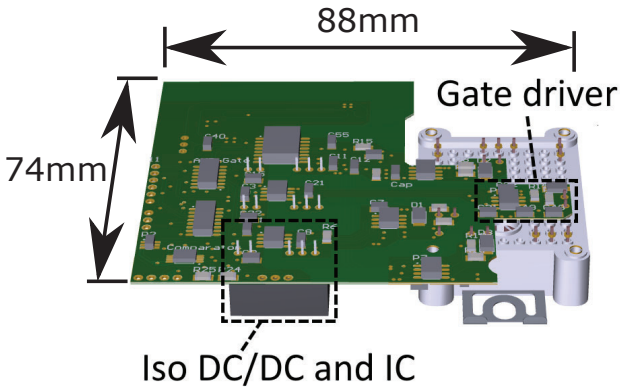

Figure 5.5: Gate driver PCB generated in a PCB designer.

5.4 Power PCB

The main functionality of the PCB is connecting the passive components to the power module. For the connection of DC-link potential the priority is a low inductive design, to minimize switch over voltage and parasitic ringing [47]. For the midpoint connected to the output filter capacitor, it is also desired to have a low inductive path. The low inductive path is desired, to obtain filter attenuation of higher frequency content. To obtain a low inductive design of the power PCB, a single layer is used as a midpoint plane, minimizing the return path. In figure 5.6 the full assembly of gate driver PCB, power PCB, power module and filtering are shown for a single phase inverter.

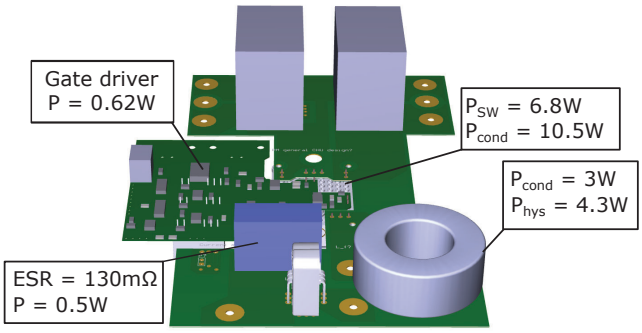

Figure 5.6: Three dimensional PCB generated in a PCB designer, with associated losses from the Pareto optimization

As can be seen from figure 5.6, the gate driver board utilizes the same surface area as the output filter. Reducing the size of the gate driver board will therefore also have a significant impact on the system power density. An investigation of a bootstrap

circuit for a T-type will therefore be conducted in the following section, together with a clarification of the advantages and disadvantages offered by the proposed circuit.

5.5 Bootstrap circuit

The circuit for a conventional bootstrap supply in a two level halfbridge converter is presented in figure 5.7. The benefit of a bootstrap circuit is the replacement of an isolated DC/DC converter with a resistor, capacitor and a diode. The capacitor is being charged during conduction of the lower switch by the DC/DC converter [48]. The bootstrap supply is particular useful for a three phase converter, as it reduces the need of four DC/DC converters to one. A disadvantages of the bootstrap is the limited modulation index. The modulation index is limited, due to requirement of periodic charging of the bootstrap capacitor to ensure safe operation. The applicability of different modulation methods are therefore restricted, as is the case for discontinuous PWM. Discontinous PWM is used to reduce the switching losses over a fundamental output period.

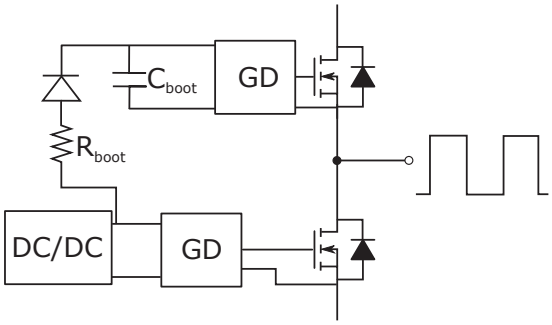

Figure 5.7: Schematic of bootstrap circuit.

Using a bootstrap circuit to power the switches in a T-type converter is also a possibility. However using the conventional bootstrap circuit supplied from a DC/DC converter connected to the lower DC-rail, severely limits the performance of the bootstrap circuit [49]. If a bootstrap circuit is supplied from the lower DC-rail, the bootstrap capacitor will only be charged during conduction of the lower switch. The lower switch only conduct during the negative half cycle of the fundamental output cycle. The charging frequency of the bootstrap circuit will as a consequence no longer be dependent on the switching frequency, but on the fundamental output frequency. Having the charging of the bootstrap circuit dependent on the fundamental output cycle will provide a lower limit of the fundamental output frequency, a physical large bootstrap capacitor and a reduction of the obtainable modulation index limit. A bootstrap charged from the bottom switch supply in a T-type is as a consequence not suitable for most applications. In the following section an alternative combination of bootstrap and isolated DC/DC converters will be presented for a T-type, Reducing the DC/DC converters count for a three phase T-type converter from seven to four.

5.5.1 Implementation of a bootstrap supply for a T-type converter

In this section, a novel bootstrap circuit is proposed for the T-type circuit. The main difference from the conventional bootstrap supply, is the connection point of the bootstrap. For the T-type the bootstrap is connected to the middle leg of the T-type converter instead of the lower DC-rail. The bootstrap supply is presented in figure 5.8

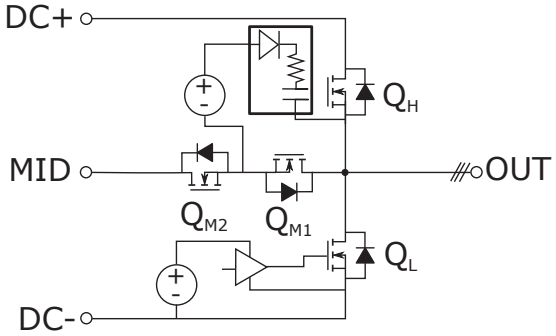

Figure 5.8: Three phase layout for a T-type of the DC/DC converter and bootstrap connections.

The advantage of connecting the bootstrap to the middle leg, is the introduction of additional charging states. Table 5.2 provides an overview of which switching states are charging the bootstrap capacitor.

Table 5.2: Charging state for a bootstrap connected to a floating source connection.

	Q_L	Q_{M1}	Q_{M2}	Q_H	Effect on C_{boot}	Charging voltage
S2	on	on	off	off	Charging	$V_{charging} = V_{cc} - V_F$
S3	off	on	off	off	Charging	$V_{charging} = V_{cc} - V_F$ if $I_{out} > 0$ $V_{charging} = V_{cc} - V_F + R_{ds-on} \cdot I_{out}$ if $I_{out} < 0$
S4	off	on	on	off	Charging	$V_{charging} = V_{cc} - V_F + R_{ds-on} \cdot I_{out}$
S5	off	off	on	off	$I_{out} > 0$ Charging, $I_{out} < 0$ Discharging	$V_{charging} = V_{cc} - V_F + R_{ds-on} \cdot I_{out}$
S6	off	off	on	on	Discharging	
S7	off	off	off	on	Discharging	
S1	on	off	off	off	Discharging	

As can be seen from table 5.2, four charging states are available. During normal operation, the active switching states are S2, S4 and S6. Switching state S2 and S4 are charging the bootstrap capacitor, compared to the conventional bootstrap circuit only including charging state S2.

During the positive fundamental half cycle the active switching states are S4 and S6. The charging of the bootstrap will as a consequence happen during the conduction of S4, which is equivalent to the charging states of a two level half bridge converter. The additional charging state introduced by the middle leg, ensures the charging frequency is dependent on the switching frequency. The proposed bootstrap circuit for a

Table 5.3: Simulation parameter used for bootstrap supply.

Parameter	Value
V_{min}	18V
C_{boot}	1μF
R_{boot}	5Ω
V_f	0.7 V
f_{sw}	50kHz
R_{ds-on}	25mΩ
f_{fund}	500 Hz
Q_g	161nC
$I_{supply+lkg}$	6mA

T-type converter will as a consequence be able to achieve an even higher modulation index limit than a half bridge converter with a small bootstrap capacitor, due to the additional voltage level introduced by the converter. The following section will quantify the performance of the bootstrap circuit, using a numerical simulation of bootstrap circuit.

Performance of bootstrap

The numerical simulation model is based on the schematic of figure 5.8. The simulation model consist of a single phase T-type converter with semiconductor models from the manufacturer, operating with a fixed junction temperature of 25°C. The parameters of the converter and bootstrap are presented in table 5.3.

For a gate driver circuit a minimum safe operating voltage is specified, to ensure the value is above the under voltage lockout limit and to prevent excessive semiconductor losses [50]. The bootstrap performance is therefore quantified by extracting the minimum bootstrap voltage during steady state operation. The two operation variables of interest when evaluating the bootstrap voltage are the modulation index and the output current. The modulation index is swept from 0.5 to 1 with output currents in the range of -30A to 30A. The simulated results of the lowest capacitor voltage as a function of modulation indexes and current is shown in figure 5.9

From the results presented in figure 5.9, a correlation between output current and bootstrap voltage can be identified. A positive output current, increases the charging voltage and as a consequence the bootstrap voltage. With a modulation index above 0.98 and 30A, the bootstrap voltage decreases rapidly. As the modulation index approaches 1, the dominant switching state is when the top semiconductor is conducting, which is not a charging state for the bootstrap capacitor. The leakage and quiescent current and the semiconductor switching will decrease the bootstrap voltage below the minimum allowed voltage, introducing a modulation index limit. The modulation index limit depends on the on-state resistance, switching frequency and output current, as it couples to the charging voltage of the bootstrap circuit [51]. Operating a T-type converter with a power factor close to one, will increase the charging voltage of the

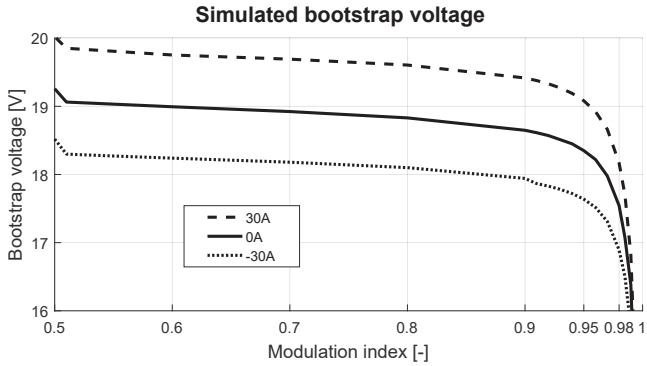

Figure 5.9: Simulated minimum bootstrap voltage as a function of current and modulation index.

bootstrap at high modulation indexes, increasing the modulation index limit for safe operation. Due to the configuration of the bootstrap circuit in a T-type converter, the interaction between the middle leg and top leg is equivalent to a conventional bootstrap in a half-bridge application. The additional voltage level in a T-type converter enables the bootstrap circuit to obtain safe operation at high modulation indexes, as is indicated by the modulation index limit of 0.98 at 30A of output current. The modulation index limits prevents the full utilization of Discontinuous Pulse With Modulation (DPWM) techniques, as they periodically clamps the output to the low or higher DC-rail to reduce switching losses [52].

The T-type converter is desired to operate with a switching frequency of 70 kHz. At that switching frequency, the switching loss account for approximately 40% of the semiconductor losses. Different DPWM techniques reducing the switching losses, could as a consequence have a substantial impact on the overall system efficiency, depending on the operation point [53].

5.6 Conclusion

An initial three dimensional layout of the power module, gate driver and power routing PCB was performed. By evaluating the geometries of the three major components, the gate driver was identified to account for a substantial surface area. The surface area of the gate driver is comparable to the area of the output filter or three times the power module area. The main reason for the large surface area of the gate driver PCB is attributed to the electrical clearance and the physical size of the isolated DC/DC converters. Based on the evaluation, a noticeable gain in power density can be obtained by reducing the size of the gate driver PCB. A new bootstrap circuit for a T-type converter was therefore proposed, to reduce the isolated DC/DC converter count from seven to four, for a three phase inverter.

The proposed bootstrap circuit, differs from conventional bootstraps by being sup-

plied from the middle leg, rather than the lower DC-rail. Using the power supply from the middle leg, increase the modulation index limit by introducing additional charging states. As a consequence a higher modulation index limit can be obtained, compared to conventional half bridge and T-type bootstrap circuits.

Decision regarding use of bootstrap

With a goal of increasing power density and reducing system cost, the T-type bootstrap circuit is an efficient solution. The disadvantages of previous and the proposed bootstrap circuit, is a modulation index limit. The modulation index limit, prevents the full utilization of different DPWM methods. For the reason of reduced flexibility in regards to PWM techniques, the bootstrap circuit will not be utilized for the prototype of the T-type converter as it is desired to maintain the degree of freedom to investigate the impact of different PWM techniques on the overall system efficiency.

CHAPTER 6

Design criteria and experimental validation

This chapter presents the extraction of parasitics for the full converter layout, with the design choices and their impact. A special focus is taken on quantifying the extracted parasitics and the local simulation performed, evaluating the performance obtained.

The paper associated with this chapter (paper D) focuses on the digital design process and the improvements obtained through design iterations.

- Paper D: Digital design of a converter using 3D models and finite element software

6.1 Introduction

With the initial design phase conducted, the next step is to evaluate the design performance. Due to the excessive di/dt and dv/dt introduced by the wide bandgap devices, the effect of parasitics are more dominant [54]. Due to the novelty of the new fast switching devices, limited practical experience is available and performing non-invasive measurements are more challenging [55]-[56]. The finite element software available today, is therefore of particular interest, as it quantifies the parasitics introduced by the layout. Parasitic extraction are therefore almost an necessity, when designing with wide bandgap devices.

The parasitic extraction also facilitates digital design iterations reducing development time and saving cost, as was mentioned in chapter 4. In relation to the digital twin, the 3D FEM extraction and local simulations are performed in this chapter. A single prototype of the power module is build to validate the performance of the power module, gate driver and power routing PCB.

6.2 Parasitic extraction using finete element software

As mentioned the parasitics were extracted for the power module, gate driver and power routing PCB. The extraction of parasitics will only be presented for the final design iterations of the components. The final layout in 3D are shown in figure 6.1 - 6.3.

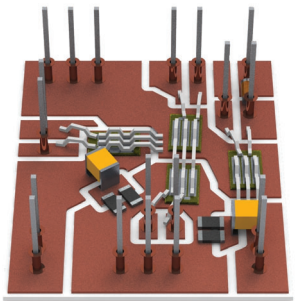

Figure 6.1: Power module

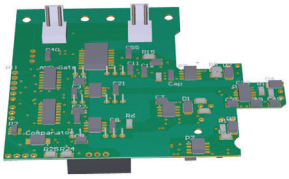

Figure 6.2: Gate driver

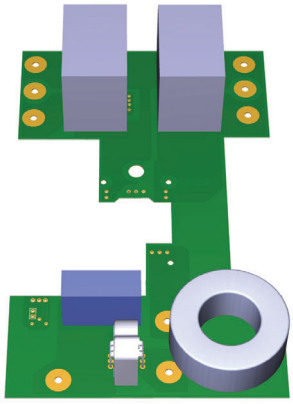

Figure 6.3: Power routing PCB

The parasitic extractions are followed by a complex local simulation, analysing the performance obtained by the layout. The local simulations utilizes the parasitics inductances, capacitances and couplings of the layout, MOSFET models from the manufacturer and models of the passive components obtained by LCR measurements.

6.2.1 Power module

The T-type converter is expected to operate with a switching frequency of 70 kHz. To operate a SiC power module at high switching frequencies, it is crucial to minimize switching losses and obtain a high efficiency. For the T-type converter, one of the challenges in obtaining low switching losses and fast switching transients are the power loop inductances. Compared to a conventional half bridge, the T-type power loop encloses three semiconductors, unavoidably increasing the power loop inductance. The increased power loop inductance worsens the switch over voltage occurring during turn-off, which also depends on the di/dt [57]. The highest di/dt obtainable during switching, can therefore be limited by the stray inductance of the power module, increasing the switching losses. A general schematic of the inductance and capacitance in the power module are presented in figure 6.4.

The extraction of the parasitics are performed using ANSYS Q3D Extractor. Figure 6.5 shows the high frequency current density from ANSYS Q3D together with table 6.1 presenting the extracted self inductance and capacitance.

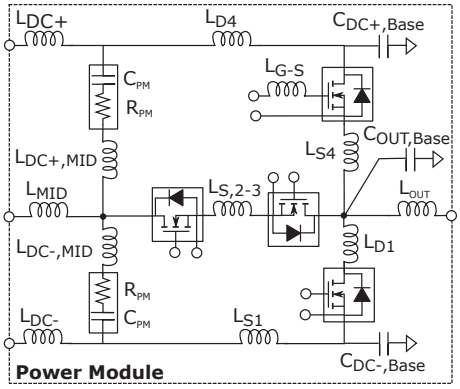

Figure 6.4: Circuit schematic of the power module designed in SolidWorks

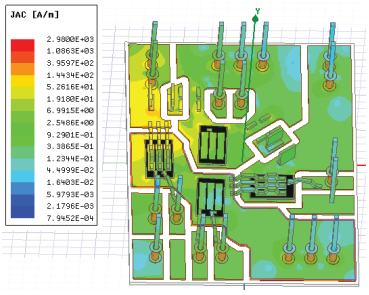

Figure 6.5: Ansys Q3D model of the power module

Table 6.1: Parasitic extracted capacitance and self inductance for the power module at 100 MHz. The mutual inductance is excluded for simplicity, but is included in the simulation model.

Parasitic	Value	Path
L_{DC+}	8.35nH	DBC + Terminal
L_{MID}	5.25nH	DBC + Terminal
L_{DC-}	5.8nH	DBC + Terminal
L_{OUT}	6.54nH	DBC + Terminal
L_{D4}	0.45nH	DBC
L_{D1}	0.57nH	DBC
L_{S4}	0.9nH	DBC
$L_{S,2-3}$	1.1nH	Bondwire
L_{S1}	1.75nH	DBC + Bondwire
$L_{MID,DC+}$	0.87nH	DBC + Component
$L_{DC-,MID}$	0.77nH	DBC + Component
$C_{OUT,Base}$	45pF	DBC
$C_{DC+,Base}$	29pF	DBC
$C_{MID,Base}$	36pF	DBC
$C_{DC-,Base}$	11pF	DBC
L_{G-S}	14.9 nH	DBC + Terminals

By comparing the magnitude of self inductances in table 6.1, a dominant contribution from power terminals can be identified. The terminal contribution is quantified by comparing the power loop inductance with and without an internal DC-link snubber. The equations for calculation the inductances are presented in equation (6.1) and (6.2), for the power loop with and without DC-link snubber respectively. The mutual inductances are excluded in the comparison, due to the low coupling coefficient associated with the power module parasitics. The purpose of the internal power module DC-link,

is to provide a low impedance between switches and DC-link, reducing switch voltage overshoot.

$$L_{with\ snubber} = L_{D4} + L_{S4} + L_{S,2-3} + L_{DC+,MID} = 3.3nH \tag{6.1}$$

$$L_{without\ snubber} = L_{DC+} + L_{D4} + L_{S4} + L_{S,2-3} + L_{MID} = 16nH \tag{6.2}$$

A factor of five in difference between the power loop inductance can be identified. A simulation is performed for the power module with and without the DC-link snubber to simulate the difference in voltage overshoot. The results are shown in figure 6.6. The overshoot voltage peaks can be identified to be 680V without and 338V with snubber. The switch over voltage without snubber is high compared to the expected blocking voltage of 280V, requiring the designer to use MOSFET with a large voltage safety margin or to reduce the switching speed of the semiconductors.

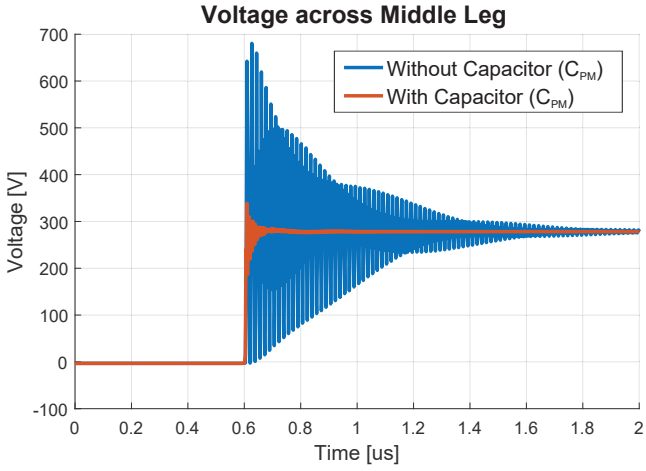

Figure 6.6: Middle switch over voltage during turn-off at 30A and 560V DC-link

Based on the simulation result in figure 6.6, the need for an internal DC-link snubber inside the power module is confirmed. Having a DC-link snubber inside the module has disadvantages. During a switching event, the voltage across the power module snubber capacitor drops. The voltage drop excites a resonance between the external DC-link capacitors placed on the power board and the power module DC-link snubber. A graphical illustration in figure 6.7 represent the resonance loop. During each switching event the resonance will be excited, creating high frequency ringing in the output voltage, introducing conducted EMI. The inductance in the resonance circuit consist of the inductance contribution from the power module terminals and the power routing PCB.

To reduce the voltage ringing and the generated EMI, a variety of solution exist. The switching speed can be reduced, to minimize the excitation of the resonance,

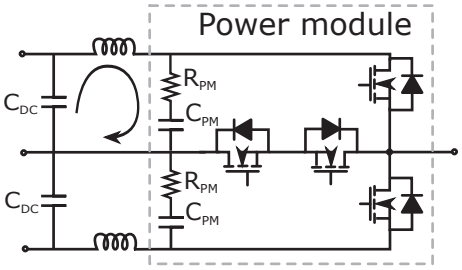

Figure 6.7: Electrical diagram, illustrating the resonance between DC-link capacitors.

however this is undesired due to the increase in switching losses. The terminal inductance can be reduced, by utilizing another terminal or packaging technology. The inductance contribution from the PCB will still be present, which account for approximately 50% of the contribution. An undamped resonance will therefore still be present in the power loop, creating undesired conducted EMI. Another solution is therefore selected, which dampens the oscillation. Damping the oscillation by introducing a resistor in the DC-link snubber, reduces the amplitude and decreases the number of ringing periods. The optimum resistance is given by (6.3) to minimize overshoot and duration of DC-link ringing [58].

$$R_{optimum} = 0.5 \cdot \sqrt{\frac{L_{stray}}{C_{pm}}} \tag{6.3}$$

With a combined inductance from power module and power routing PCB of 28 nH and a power module capacitance of 50 nF, an optimum damping resistor of 0.28 Ω is calculated. The actual optimum resistance is obtained by subtracting the ESR of DC-link capacitors and parasitic resistance of the layouts from the value calculated. The DC-link snubber voltage ringing with and without damping can be seen in figure 6.8.

As can be seen from figure 6.8, the damped resonance oscillates for two periods before settling. The performance of the selected damping resistor is validated. Utilizing a DC-link snubber with a damping resistor reduces the switching over voltage and dampens parasitic ringing, improving the switching transients. Based on the two local simulations, the performance of the power module and power routing PCB is confirmed. The remaining layout to evaluate is the gate driver design.

6.2.2 Gate driver PCB

Compared to the full gate driver circuit including among other components digital isolators, DC/DC converters and IC, the parasitics of interests are present in the gate driver Gate-Source loop. To reduce simulation time and complexity of the exported parasitics, a section of the 3 dimensional layout containing the gate driver IC and resistors are imported into ANSYS Q3D Extractor. The gate driver and the extracted parasitics are presented in figure 6.9 and table 6.2

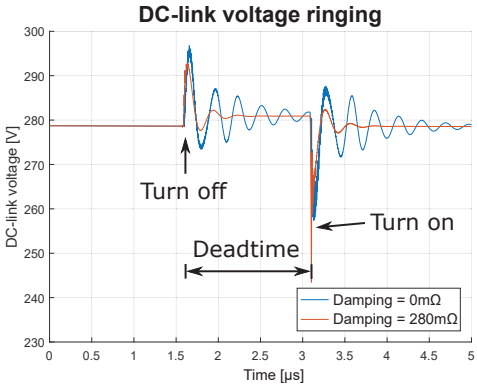

Figure 6.8: Simulated voltage ringing of the power module capacitor between MID and DC+ potentials, during switching.

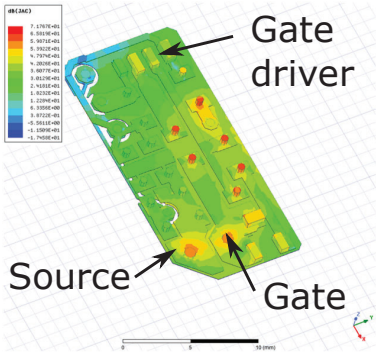

Figure 6.9: Ansys Q3D model of gate driver

Table 6.2: Gate driver parameter including parasitics

Parameter	Value
V_{CC+}	20V
V_{CC-}	−5V
R_{on}	5Ω
R_{off}	2Ω
L_{on}	5.2nH
L_{off}	3nH
L_{G-S}	14.9nH
C_{iss}	2.8nF
R_{int}	1.1Ω
V_{GSmax}	25V
V_{GSmin}	−10V

The performance criteria of interest for the gate driver is the voltage overshoot and undershoot cause by turn on and off, and the voltage overshoot cause by the miller effect. Firstly the inductance is extracted from the PCB, an inductance value of 5.2nH and 3nH are obtained during turn on and off respectively. The analytical equations for a LCR circuit is used to calculate the overshoot and undershoot with a gate resistance of 5Ω during turn on and 2Ω during turn off. The parameters used for inductances, resistances, capacitances and voltage limits are shown in table 6.2.

$$\frac{V_{GS}(s)}{V_o} = \frac{\frac{1}{L_{EQ} \cdot C_{iss}}}{s^2 + \frac{R_{EQ}}{L_{EQ}} \cdot s + \frac{1}{L_{EQ} \cdot C_{iss}}} \tag{6.4}$$

$$\zeta = 0.5 \cdot R_g \cdot \sqrt{\frac{C_{iss}}{L}} \tag{6.5}$$

With the equation presented in (6.4) and (6.5), it is shown that no voltage overshoot is present during turn on and an undershoot reaching -8.5V is present during turn off. These values are within the safety margin presented in table 6.2. The initial investigation validates the voltage overshoots being within the limits of the SiC MOSFET die. Decreasing the turn off resistance further, would result in a voltage undershoot below the limit value. The next step is to verify, the off resistance, being low enough to prevent false turn on caused by the miller current. To simulate the Miller effect, the full model complexity is used. The model includes parasitics extraction from power module, gate driver and power routing PCB. A local picture of the LTspice gate driver model is shown in figure 6.10. The simulation result is shown in figure 6.11.

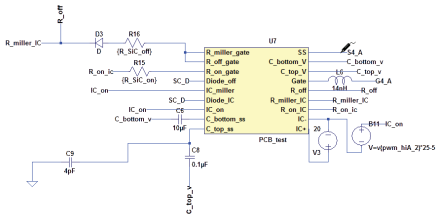

Figure 6.10: LTspice model of the gate driver

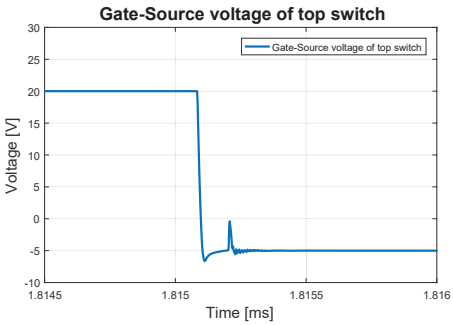

Figure 6.11: Simulate Miller effect for top switch, under high dV/dt conditions.

As shown in figure 6.11, the voltage reaches -0.5V when the complementary switch is turned on. The threshold is typically 2.6V [59], meaning a sufficient safety margin is present. The gate driver design is validated in regards to overshoot and false turn on immunity. The largest contributor of gate-loop inductance is the power module terminals. Optimizing the gate driver PCB further will as a consequence have an insignificant impact on the switching performance.

6.2.3 System parasitic

Based on the parasitics extracted from the power module, power routing PCB and gate driver PCB, a simplified overview of the parasitic contributions are presented in figure 6.12, with the parasitic values quantified in table 6.3.

Based on the parasitic extractions, a full converter simulation is developed. The full converter model is capable of simulating the switching transients, and will be used for experimental validation in the following section.

6.3 Validation of simulation

With the performance of the layout thoroughly investigated using digital simulations, a prototype of a single phase power module is build. The single phase converter will

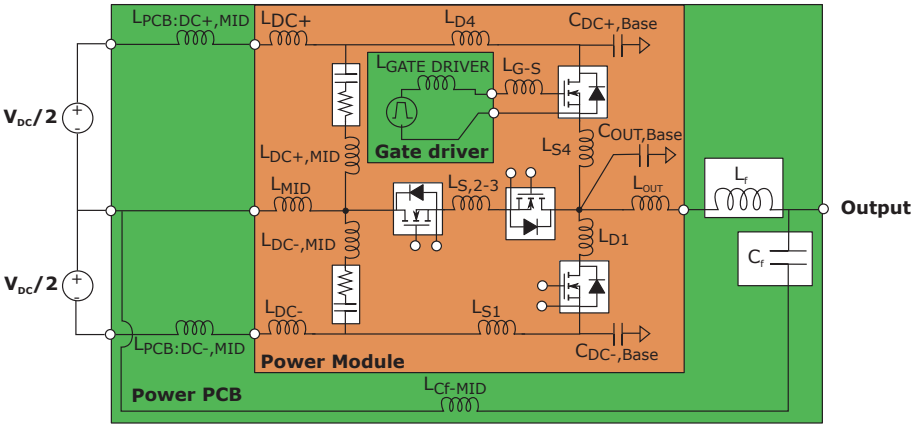

Figure 6.12: Power module designed in SolidWorks

Table 6.3: Extracted parasitics of power module and PCB boards at 100 MHz.

Parasitic	Value	Path
L_{DC+}	8.35nH	DBC + Terminal
L_{MID}	5.25nH	DBC + Terminal
L_{DC-}	5.8nH	DBC + Terminal
L_{OUT}	6.54nH	DBC + Terminal
L_{D4}	0.45nH	DBC
L_{D1}	0.57nH	DBC
L_{S4}	0.9nH	DBC
$L_{S,2-3}$	1.1nH	Bondwire
L_{S1}	1.75nH	DBC + Bondwire
$L_{MID,DC+}$	0.87nH	DBC + Component
$L_{DC-,MID}$	0.77nH	DBC + Component
$C_{OUT,Base}$	45pF	DBC
$C_{DC+,Base}$	29pF	DBC
$C_{MID,Base}$	36pF	DBC
$C_{DC-,Base}$	11pF	DBC
L_{G-S}	14.9 nH	DBC + Terminals
$L_{Gate\,driver}$	2.9 nH	PCB
$L_{PCB:DC+,MID}$	14.5 nH	PCB
$L_{PCB:MID,DC-}$	14.7 nH	PCB
$L_{Cf:MID}$	39.6 nH	PCB

be used for a double pulse setup, validating the switching performance. The power module and the double pulse setup are shown in figure 6.13 and 6.14 respectively.

A T-type can be configured to perform a double pulse, by continuously conducting

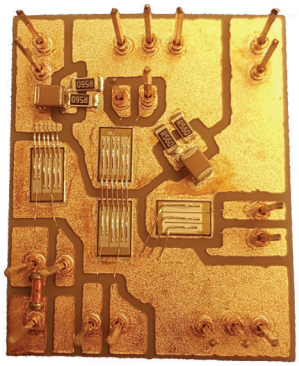

Figure 6.13: Photograph of the power module.

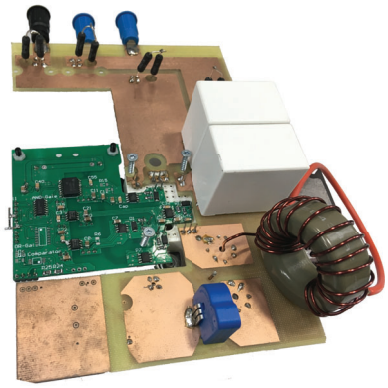

Figure 6.14: Photograph of the double pulse seetup.

one of the middle leg switches. The T-type converter then becomes equivalent to a half bridge converter with half the DC-link voltage. The inductor is then connected to a DC-link node, depending on which semiconductor is being actively switched.

6.3.1 Experimental measurements

Experimental measurement are shown when actively controlling the top side switch. The double pulse test is performed with a DC-link voltage of 560 V and an inductor current of 30 A. During normal operation, the converter is expected to operate with a RMS current of 16 A, equivalent to a peak current of 22.5 A. Validating the performance with an inductor current of 30 A is therefore sufficient to verify the switching performance during normal operation. The measured and simulated double pulse waveforms are shown in figure 6.15

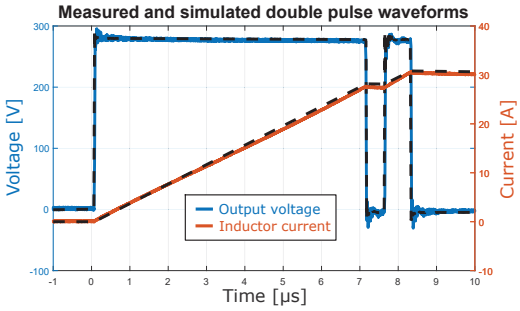

Figure 6.15: Simulated and measured inductor current and output voltage during double pulse test. The solid lines are measured and the dashed are simulated.

Comparing the simulated and measured response in figure 6.15, an excellent agree-

ment is observed when considering the μs scale. The low frequency ringing seen in both the measured and simulated response, is the ringing introduced by the DC-link resonance. The measured waveforms confirms the selection of a suitable damping resistor, dampening the oscillation after two ringing periods. As the T-type power module has an internal DC-link, the semiconductor current can not be measured using the DC-link terminals. The turn on and turn off voltage output is therefore analysed with a timescale of ns, to compare the simulated and measured switching transients. The comparison between measured and simulated output voltage during turn on and off are shown in figure 6.16. When the top switch is turned on the output voltage rises to $V_{DC}/2$ and during turn off the output voltage drops to 0, being the midpoint potential.

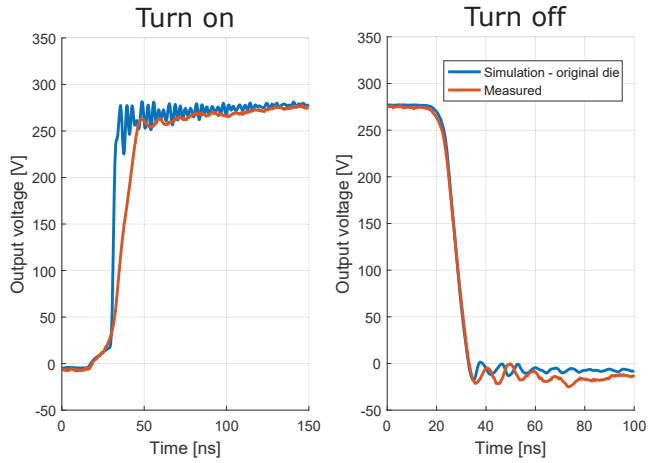

Figure 6.16: Turn on and off with a DC-link voltage of 560V and 30A of inductor current

By comparing the turn on transients, a difference can be identified in the rise time of the voltage, and as a consequence the dV/dt. The simulation model estimates a dV/dt of 52 kV/μs compared to the measured of 14 kV/μs. The turn on waveform depends on the device characteristics, parasitic capacitance, inductances and gate resistance. The explanation of the deviation is therefore expected to be caused by detail mismatch in one of the above.

During turn off, the simulated and experimental measured waveforms are in almost perfect agreement. The turn off waveform depends on the inductor current and the parasitic and device capacitance, where the latter is dominant. Based on the perfect agreement between measurement and simulation, the modelled and actual device capacitance are expected to be in good agreement.

Until this point, it was assumed that the MOSFET model, which was supplied by the manufacturer, was an accurate representation of the physical semiconductor devices. The experimental measured turn on questions the validity of this assumption, and as a consequence the characteristics between the measured and simulated semi-

conductor dies are investigated in the following section.

6.3.2 Semiconductor model deviation

The approach used to compare the semiconductor model with the physical devices, is by extracting the device capacitance and the IV-characteristics of the device. For the physical semiconductor a curvetracer is used to measure the MOSFET characteristics. An equivalent curvetracer is build in LTspice extracting the curves and parameters from the semiconductor model. The measured and extracted semiconductor model IV-characteristics are shown in figure 6.17. As can be seen a substantial difference is present in the IV-characteristics.

The threshold voltage of the physical semiconductor is approximately 2V higher than the model threshold, resulting in a reduce voltage across the external and internal gate resistor. The reduced voltage across the gate resistor reduces the charging current during the miller plateau by 20%, a 20% dV/dt deviation can as a consequence be allocated solely to the variation in threshold voltage.

Further more, the slope at high V_{DS} does not match, as is identified by comparing the characteristics of V_{GS} = 8V from simulation to V_{GS} = 10V of measurement. This is a critical observation, as the V_{DS} dependency of the IV-characteristics are crucial during a switching transients, as it determines the miller plateau. The fact that the measured IV-characteristics with a low value of V_{DS} does not match the simulated behaviour, results in a high degree of uncertainty associated with the switching transient. The simulated and measured channel resistance are in good agreement, coherent with the correlation between simulation and measurement in the μs range.

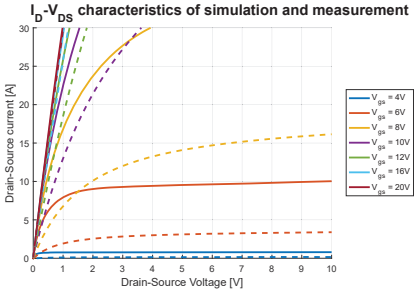

Figure 6.17: IV-characteristics of the SiC MOSFET. The dashed line is measured IV characteristics and the solid line is extracted from the simulation model.

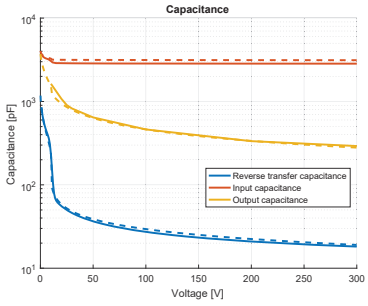

Figure 6.18: Comparison between measured and simulated device capacitance. Solid line is simulated and dashed is measured capacitance.

By comparing the measured and simulated device capacitance in figure 6.18, an excellent agreement can be observed. The good agreement was also expected as the turn off waveforms for simulation and measurement were identical which depends on the device capacitance, parasitic capacitance and output current.

Based on the comparison of the model semiconductor deviation, the capacitance and channel resistance are in good agreement, as was expected from the double pulse

test. However substantial deviation in the IV-characteristics are observed, resulting in a large uncertainty related to the Miller plateau at higher V_{DS} voltages and the switching trajectory [60]. A refined model of the semiconductor is therefore needed if the switching losses are desired to be estimated with a high degree of accuracy.

6.4 Conclusion

Based on the digital twin, an accurate representation of the full converter system was build, including the layout parasitics. The layout was evaluated using complex local simulation, quantifying the performance obtained. After a vast amount of design iterations a layout with a satisfactory performance was obtained. A single phase converter was build based on the final design and the performance was validated. Based on the parasitic extraction of the power module, gate driver and power routing PCB, the dominant contribution of parasitic are the power module terminals. It is therefore crucial to address the impact of terminals, when designing a converter with wide bandgap devices. To circumvent the terminal inductance in the power loop, an internal DC-link snubber is placed inside the power module. The DC-link snubber reduces the voltage overshoot during turn off, enabling fast switching. The clean switching transient was confirmed by experimental measurements, with no noticeable voltage overshoot. The terminals also dominates the gate-loop inductance contribution. Design iterations of the gate driver layout are therefore not prioritized, due to the limited effect on gate-source voltage under/overshoots. By comparing the simulation results from the digital model and the measured waveforms, a good agreement was observed in the μs range. When comparing the switching transient on a ns scale, deviation was observed in the turn on transient. The root cause of the deviation can be explained by the discrepancy in the IV-characteristics between the physical MOSFET die and the model provided by the manufacturer. A good agreement of the device capacitance were observed between the MOSFET model and the physical device, which is compatible with the perfect agreement in measured and simulated turn off behaviour.

CHAPTER 7

From switching transients to system simulation

This chapter will present the design of a system simulation based on the information generated by complex local simulations. The full system simulation will be validated by building and performing measurements on a three phase T-type converter.

The paper associated with this chapter (Paper E) focuses on the three phase T-type inverter system optimized for high switching frequencies. In the paper the total total harmonic distortion (THD) was calculated for the load current, validating a THD below the target limit of 5% was achieved.

- Paper E: Fast Switching T-type Converter based on SiC MOSFETs for Drive Applications

7.1 Introduction

When performing a simulation of the full converter system, it is desired to simulate among other things controller stability, current inrush, power dissipation, average temperature and temperature swings. Due to the slow response associated with for example temperature increase, a simulated time period of several second or minutes are needed to reach steady state conditions [61]. The developed local simulation models typically simulates a few switching transients at a specific operation point, in the nanosecond to microsecond range. Extending the time simulated for the local simulation will increase the execution time of the simulation dramatically, as the local simulations are designed to have a high degree of accuracy during switching transients. Even simulating a few fundamental output cycles becomes extremely time consuming and impractical, when the local models are used. A model is therefore needed which utilizes the high quality information obtained from the local simulations and is capable of simulating minutes of operation. Based on the desired output of the system simulation, an appropriate simulating software is selected. For this project PLECS is selected, as it supports implementation of a thermal network together with the semiconductor losses using a look-up table. The overall flow diagram of the information passed from local simulations to the system simulation are presented in figure 7.1.

The power loss look-up table will be generated using the local simulation models build in LTspice. The thermal network will be extracted from a thermal simulation in COMSOL, which will be presented in section 7.3. How the information are exported from the local to the system simulation is divided into two sections, covering the electrical and thermal modelling.

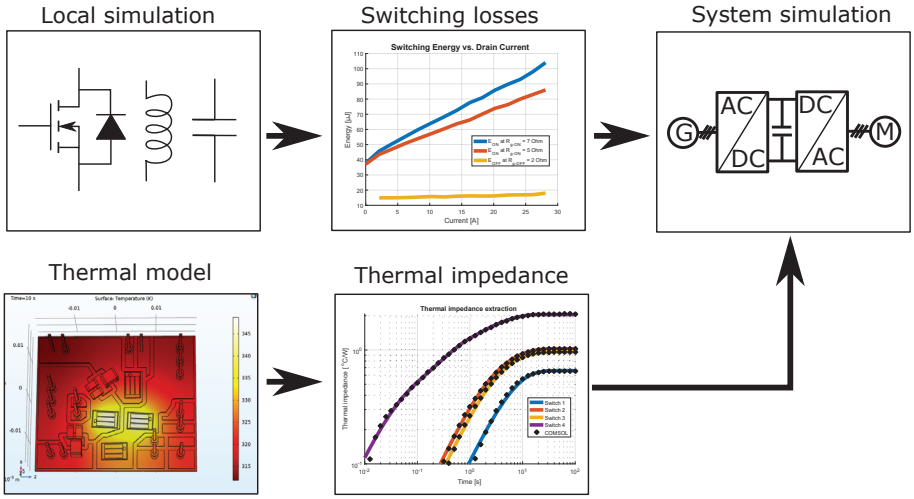

Figure 7.1: Flowchart of the information exported from local simulation models to the system simulation

7.2 Electrical Model

The two major sources of informations exported are the switching losses from the LTspice simulation including parasitics and semiconductor models, and the modelling of the output filter. The first section will present the filter design and modelling, where the second section will cover the exported switching losses.

7.2.1 Filter design

The output filter selected in section 3.2.3, was a LC-filter. The neutral point of the filter capacitors are connected to the midpoint of the DC-link, ensuring differential and common mode filtering. For the output filter an inductor of 430μH at 0 A and a capacitor of 1μF was selected. The cutoff frequency of the filter is 7.7kHz, which is close to the logarithmic mean of the highest fundamental output frequency and the switching frequency. Designing a filter with a cuttoff frequency at the logarithmic mean ensures a low distortion of the fundamental output frequency and a high attenuation of the switching frequency. As the output capacitor is a prespecified commercial capacitor, a special focus will be on the winding of the inductor. Principal schematics of the output filter is shown in figure 7.2 with and without parasitic contributions.

When designing an inductor for a converter utilizing wide bandgap devices, a special focus is on minimizing the parallel capacitance C_L, which introduces a low impedance current path at higher frequencies. The parallel capacitance increases the switching losses of the converter and worsens the EMI performance. The parasitic parallel capacitance is a combination of the capacitive coupling between turns, and from core to windings [62]. With the goal of minimizing the parallel capacitance, the

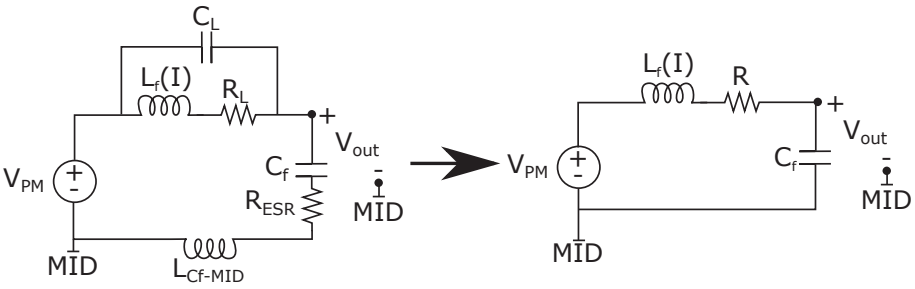

Figure 7.2: Impedance model of the output filter with and without parasitic contributions.

inductor windings should have a low potential differences between the windings in near proximity. The capacitive contribution from winding to core can be reduced by increasing the wire isolation or by introducing spacing between winding and core. The winding methods utilized to reduce the coupling capacitance, is graphically illustrated in figure 7.3. The first and last windings are physical spaced apart.

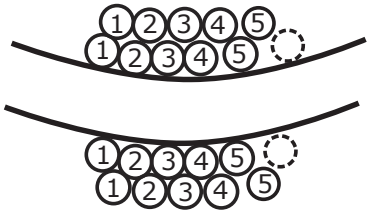

Figure 7.3: Winding method applied on the filter inductor, to reduce the magnitude of the parasitic parallel capacitance. The method is illustrated with two parallel wires.

With the inductor designed, the modelling complexity of the filter should be selected, for the system simulation. The impedance of the inductor and capacitor are presented in equation (7.1). The output transfer function is simplified in equation (7.2), by neglecting the parallel coupling capacitance C_L and the stray inductance L_{Cf-MID}.

$$Z_{L_f} = \frac{\frac{1}{C_L}\cdot s + \frac{R_L}{C_L \cdot L_f}}{s^2 + \frac{R_L}{L_f}\cdot s + \frac{1}{L_f \cdot C_L}} \quad , \quad Z_{C_f} = \frac{L_{Cf-MID}\cdot s^2 + R_{ESR}\cdot s + \frac{1}{C_L}}{s} \tag{7.1}$$

$$G_{filter} = \frac{V_{out}(s)}{V_{PM}(s)} = \frac{Z_{C_f}}{Z_{C_f} + Z_{L_f}} \approx \frac{\frac{R_{ESR}}{L_f}\cdot s + \frac{1}{L_f \cdot C_f}}{s^2 + \frac{R_{ESR}+R_L}{L_f}\cdot s + \frac{1}{L_f \cdot C_f}} \tag{7.2}$$

The response of the transfer function presented in equation (7.2) is shown in figure 7.4 with and without the parasitic contribution. The response is obtained using the information from ANSYS Q3D extractor and the impedance measurements performed on the output filter.

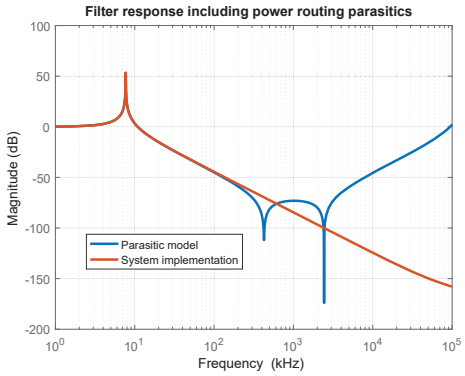

Figure 7.4: Filter response at an output current of 0 A.

As can be seen from figure 7.4, the parasitic impacts the higher frequency response of the filter. As the switching speed of the wide bandgap devices increase, the frequency content associated with the transients increases. It is therefore of higher importance to address the parasitics in the design phase [63]. However as seen from the bode diagram, at frequency below 300 kHz no substantial deviation between models can be observed. The simplified filter model therefore accurately represents the filter response for frequencies upto the switching frequency. The dV/dt introduced by a simulation software as PLECS depends on the step size in the simulation, as the transistor is only defined as either on or off. The dV/dt is therefore no longer associated with the operation of the physical device, but only on the simulation settings. The frequency content generated and therefore the response of the parasitics are as a consequence no longer a representation of its real behaviour in the system. High frequency parasitics should therefore be avoided in system simulation software as PLECS. The simple model introduced in figure 7.2 and in equation (7.2) will therefore be used in the system simulation.

7.2.2 Export of switching losses

Due to the internal DC-link of the power module described in chapter 6.2.1, the switch current and voltage can not be measured directly during a double pulse test without removing the housing. It is, as a consequence, not possible to experimentally determine the switching losses without modifying the power module. The switching losses are as a consequence determined based on the complex local simulation model developed in section 6.3. To extract the switching losses, multiple double pulse tests are simulated with a current step size of 2 A and a junction temperature of 25°C. The extracted switching losses are presented in figure 7.5 with a turn on gate resistance of 7Ω or 5Ω and a turn off gate resistance of 2Ω. In practice a 7Ω turn on and 2Ω turn off gate resistor are utilized.

Combining the extracted switching and conduction losses, the power dissipation of the semiconductors can be calculated, and used as an input for the thermal simulation.

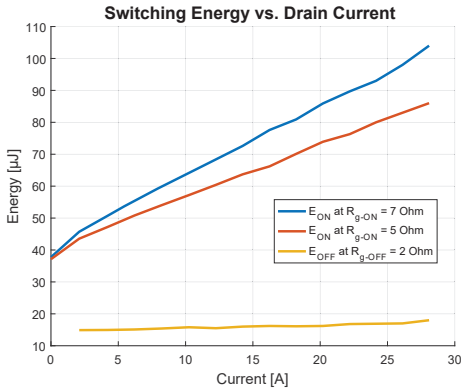

Figure 7.5: Switching losses extracted from LTspice simulation including layout parasitics.

7.3 Thermal Model

The thermal performance of a power module is critical to model, for identifying a power dissipation limit for the semiconductors. The combination of a thermal and electrical model allows the designer to estimate device temperatures during operation. The electro-thermal model can then be used for identifying potential over temperatures during operation and for reliability assessments. To develop a thermal model a three-dimensional drawing of the power module is needed together with the material properties. The 3D layout was previously used in section 6.2, easing the transition into the thermal simulation. The thermal properties of the power module are found by a literary search, the properties are presented in table 7.1 [64].

Table 7.1: Thermal properties of the materials used for the thermal simulation.

Material	Thermal Conductivity	Heat Capacity	Density
SiC	120 $\frac{W}{m \cdot K}$	675 $\frac{J}{kg \cdot K}$	3160 $\frac{kg}{m^3}$
Solder	64 $\frac{W}{m \cdot K}$	230 $\frac{J}{kg \cdot K}$	7350 $\frac{kg}{m^3}$
Aluminium	238 $\frac{W}{m \cdot K}$	900 $\frac{J}{kg \cdot K}$	2700 $\frac{kg}{m^3}$
Copper	400 $\frac{W}{m \cdot K}$	385 $\frac{J}{kg \cdot K}$	8960 $\frac{kg}{m^3}$
AlN	170 $\frac{W}{m \cdot K}$	745 $\frac{J}{kg \cdot K}$	3260 $\frac{kg}{m^3}$

The reason for not including the gate driver and power routing PCB in the thermal simulation, is due to the physical separation performed by the terminals. The power module terminals are placed mainly at the edges of the power module, where as the semiconductors dissipating power are placed in the center. The distance between semiconductor dies and terminals, the height of the terminals and the poor heat trans-

fer from PCB to air introduces a neglectable thermal coupling to ambient, which do not affect the result [65]. The thermal impedance and couplings of the semiconductor dies are obtained by extracting the average surface temperature of the die, subtracting the ambient temperature and diving by the power dissipation, as shown in equation (7.3). Z_{S-i} is the thermal impedance and ψ_{th-ij} is the thermal coupling of the dies.

$$Z_{S-i} = \frac{T_{junction-i} - T_{amb}}{P_i} \quad , \quad \psi_{th-ij} = \frac{T_{junction-j} - T_{amb}}{P_i} \tag{7.3}$$

The thermal impedances and couplings can be put on a matrix form as shown in equation (7.4) representing the thermal response of the system.

$$\begin{bmatrix} T_{S1} \\ T_{S2} \\ T_{S3} \\ T_{S4} \end{bmatrix} = \begin{bmatrix} Z_{S1} & \psi_{S1,2} & \psi_{S1,3} & \psi_{S1,4} \\ \psi_{S2,1} & Z_{S2} & \psi_{S2,3} & \psi_{S2,4} \\ \psi_{S3,1} & \psi_{S3,2} & Z_{S3} & \psi_{S3,4} \\ \psi_{S4,1} & \psi_{S4,2} & \psi_{S4,3} & Z_{S4} \end{bmatrix} \cdot \begin{bmatrix} P_{S1} \\ P_{S2} \\ P_{S3} \\ P_{S4} \end{bmatrix} + T_{amb} \tag{7.4}$$

To ensure the steady state temperature was reached, a simulated time of 100 s is utilized with a logarithmic step size. The logarithmic step size ensures a high accuracy in the initial fast thermal response, as well as reducing the data points for the slower thermal response. For the thermal simulation a heat transfer coefficient of 1000 $\frac{W}{m^2 \cdot k}$ is assumed for the heatsink. The simulated temperature distribution after 100 s is shown in figure 7.6, with switch S1 dissipating 20W of power. As can be identified from figure 7.6 a temperature increase can be identified for the surrounding switches, validating a thermal coupling between semiconductors is present.

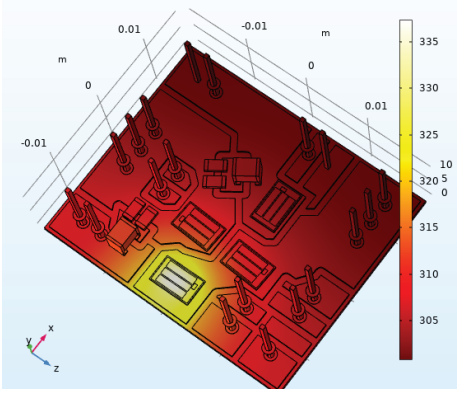

Figure 7.6: Simulated surface temperature of the power module, without bondwires.

Using equation (7.3), the thermal impedance can be calculated based on the extracted temperature over time, as shown in figure 7.7.

A third order foster network is fitted to the thermal impedance from COMSOL. The foster network fit is presented in figure 7.7, validating a high modelling accuracy is obtained. The procedure is repeated for all semiconductors. The results is a third

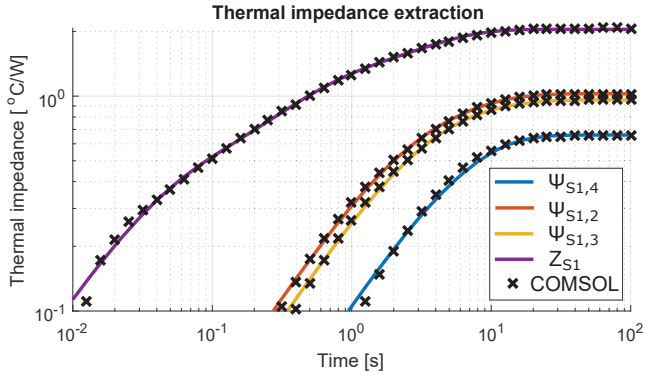

Figure 7.7: Thermal impedance extracted from the thermal simulation.

Table 7.2: Fitted thermal impedance of the semiconductor switches.

Thermal impedance	First order		Second order		Third order	
	R1 [K/W]	C1 [W·s/K]	R2 [K/W]	C2 [W·s/K]	R3 [K/W]	C3 [W·s/K]
Z_{S1}	0.3415	0.09389	0.7502	0.5229	0.9539	3.605
Z_{S2}	0.4108	0.09448	0.5191	0.7108	0.8104	5.469
Z_{S3}	0.4124	0.09439	0.5207	0.7497	0.8469	5.037
Z_{S4}	0.3864	0.09761	0.5011	0.5909	0.8741	4.342

order foster network for each thermal impedance and coupling term in the matrix presented in equation (7.4). The fitted parameter for the thermal impedance of each switch is presented in table 7.2.

7.3.1 Simulated device temperature

Combining the thermal network with the switching losses in the look-up table and an on-state resistance, the junction temperature of the dies are simulated. The junction temperatures are simulated with an output current of 16 A, a fundamental frequency of 19 Hz and an output power of 7.5 kW. The temperature variation off all semiconductor dies are presented in figure 7.8 for six fundamental cycles.

As seen from figure 7.8 switch S1 reaches the highest temperature of 38.5°C. The higher junction temperature for switch S1 is associated with the thermal spread being limited by the DBC edge, as was shown in figure 7.6. The reduced thermal spread increases the thermal impedance from switch S1 to ambient. A maximum temperature swing of 1.5°C with an average temperature of 37.7°C validates the low thermal impedance obtained by the power module. The low thermal impedance is obtained by the combination of four semiconductor dies per phase, distributing the power dissipation during a fundamental cycle and the use of AlN ceramic, increasing the thermal

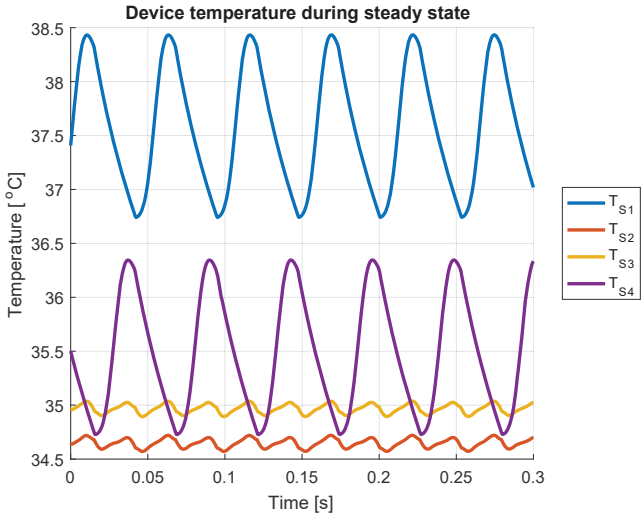

Figure 7.8: Simulated junction temperature in PLECS after 30 seconds, ensuring steady state.

conductivity of the power module. With the low temperature swings and average temperature obtained, the thermal performance of the power module is validated. Based on the thermal simulation, only small temperature increase are therefore expected when performing experiments.

7.4 Experimental measurements of the three phase converter

With the junction temperature simulated, the next step is to build a three phase converter and to validate the electrical performance, considering a fundamental output cycle. Additional power modules where manufactured as shown in figure 7.9 and a full three phase converter was build as shown in figure 7.10

A custom DSP interface card was build for the three phase setup, including DC-link voltage measurement, filtering of measurements and a gate driver buffer enabling safe start-up. The DSP interface card is not represented in figure 7.10 and will not be presented in detail. The filtering of the voltage and current measurements performed by the interface card is included in the system simulation, taking into consideration the impact on control.

7.4.1 Three phase measurements

For the three phase experiment, two DC-link voltage sources were used to supply power to the DC-link. A three phase resistor was connected at the converter output,

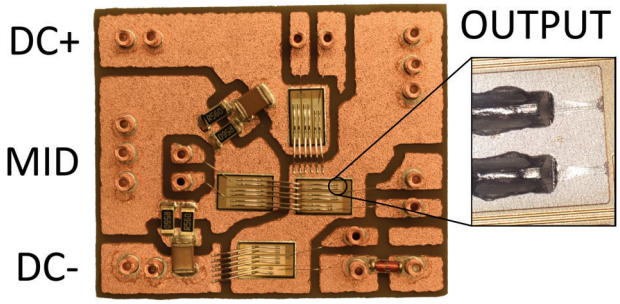

Figure 7.9: Single phase power module with a zoom in focus on the bondwire.

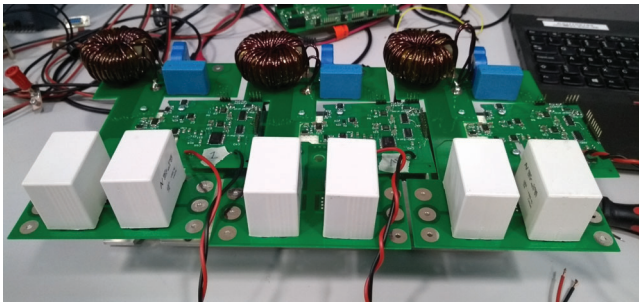

Figure 7.10: Picture of the three phase converter.

acting as a load. The load resistor limited the output current of the converter to 10 A RMS, which is 63% of the intended RMS current. However the setup is sufficient to demonstrate stable operation with a switching frequency of 64 kHz, a DC-link voltage of 560V and an output RMS current of 10A.

To validate continuous switching of the power module and acceptable inductor current ripple, the output current and voltage of the power module were measured. The measured waveforms are shown for a single fundamental cycle in figure 7.11 and a zoomed view of the inductor current and power module voltage in figure 7.12.

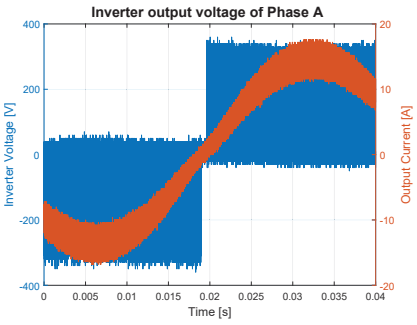

Figure 7.11: Measured inductor current and inverter voltage

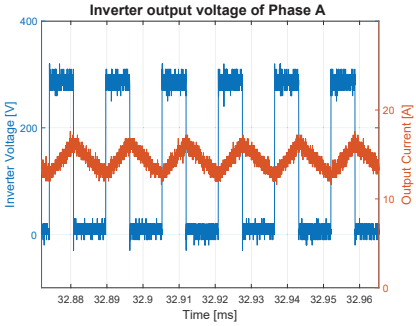

Figure 7.12: Zoom of voltage and current measurements.

From the two figures, it can be seen that no voltage overshoot are present during a fundamental cycle. The zoom of the inductor current is taken at an average current of 14.4 A with a current ripple of 3.2 A. Which is in perfect agreement with the simulated filter response as shown in figure 7.13. The accurate representation of the inductor current, validates the modelled current dependency of the inductance.

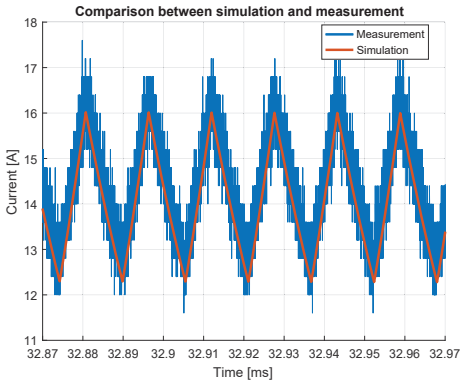

Figure 7.13: Comparison between simulation and measurement

With the modelling of the inductor and the continuous switching validated, the next step is to validate the LC-filter attenuation. The filter attenuation of the switching frequency and its harmonics are of particular interests, as it evaluates on the performance obtained by the designed filter. Quantifying whether a larger attenuation and thereby larger filter volume is needed. To evaluate on the harmonic content of the output waveforms, the output current is measured with a resistive load. As a resistive load is utilized the harmonic content of the current is comparable with the differential mode harmonics in the output voltage. The measured output current is shown in figure 7.14 together with a discrete Fourier transformation of the signal. The sampling window corresponds to a single fundamental output period of 19 Hz.

As can be seen from figure 7.14, a high attenuation of the switching frequency and

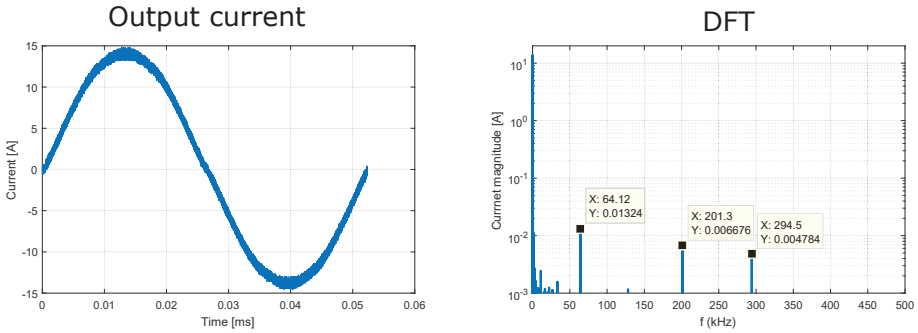

Figure 7.14: Measured load current and DFT of the high frequency harmonics.

its harmonics are obtained [66]. The fundamental amplitude of the output current is 14 A, meaning a switching frequency content of 13 mA only contribute with a minor distortion of the fundamental signal. The amplitudes of the switching frequency and its harmonics in figure 7.14 validates, that a sinusoidal output current is obtained with an output inductor of only 60cm^3, per phase. Increasing the switching frequency beyond 64 kHz will only have an small impact on the filter size and most likely increasing the overall system volume. The system volume would increase due to the increased cooling requirements or due to the faster switching transients increasing the size of the input EMI filter [63], [67]. The penalty of increasing the switching is in alignment with the findings of the pareto optimization algorithm in chapter 3, presenting 64 kHz to be the limiting switching frequency for achieving high power densities.

7.5 Conclusion

Using the information from local simulations, an electro-thermal system simulation was developed. The system simulation utilized the extracted switching losses from LTspice and the thermal network extracted from COMSOL. The system simulation extends the time period simulated from a few micro seconds to several seconds of operation. Based on the system simulation the thermal performance of the power module was evaluated. A very low average temperature increase and low temperature swings were simulated under normal operating conditions, validating the thermal performance of the power module. A three phase experimental setup was developed for the three level converter, to evaluate the electrical performance achieved. The performance of the output filter was simulated using the system simulation and experimental validated by measuring the inductor current and the output voltage of the power module. The measured and simulated waveforms were in perfect agreement. To validate the high power density obtained by the converter, the load current was measured and the harmonic content were evaluated. Based on the measured load current a very high attenuation of the switching frequency and its harmonics were obtained. The load current measurement confirms that a sinusoidal output current is obtained with only

$60cm^3$ of inductor per phase, enabling a high converter power density.

CHAPTER 8

Conclusion

The purpose of this chapter, is to summaries the conclusions provided throughout the Ph.D. thesis. The aim of the thesis is to provide methods of designing and building a converter with a high power density and efficiency, using the new wide bandgap devices.

To identify the components which limits the power density and efficiency of existing converters, a commercially available power converter was disassembled and the volume of the major components were quantified. Based on the disassembly the input and output filter were identified to account for 74.5% of the volume, 9% was contributed by the heatsink, 5.1% from control and only 0.6% of the power module. Based on the volume distribution it becomes apparent, that the major components which volume should be reduced to increase power density are the heatsink and filter volume. The reason for the large filter and heatsink size is related to the relative high switching losses associated with Si semiconductor, limiting the obtainable efficiency and switching frequency.

To design a converter using the new wide bandgap devices with high power density and efficiency, a research question related to the optimum selection of converter topology, semiconductors and switching frequency becomes crucial to answer. Due to the limited experience with wide bandgap semiconductor and the large complexity related in considering the interaction between system components, answering this question objectively using hand calculations is nearly impossible. A multi objective Pareto algorithm was therefore developed with an extensive level of detail, evaluating power density, efficiency and cost using analytical equations and commercially available components. The results extracted from the algorithm was obtained by evaluating topologies ranging from a half bridge (two level) to a Pi-type (four level) converter with switching frequencies ranging from 25 kHz to 150 kHz.

The results showed that the conventional half bridge topology achieve a lower efficiency and power density compared to the more advanced topologies. The half bridge is substantially cheaper in manufacturing costs compared to other topologies which is the justification of why it is the most common topology used in commercial products. By prioritizing efficiency and power density, the T-type converter obtains the power density and efficiency increase at a substantial lower cost, compared to its multilevel alternatives. By considering power density, efficiency and cost a T-type converter was as a consequence selected as the optimum topology for the specific application. The results from the Pareto algorithm identifies a switching frequency of 70 kHz to obtain the highest power density with an efficiency above 99 %.

Due to the fast switching transients associated with the new wide bandgap devices, the parasitic introduced by the layout will have an increased impact on the system performance. It is therefore critical to understand what circuit elements introduces the dominant parasitics, in order to optimize the converter layout for wide bandgap devices. A finite element software named ANSYS Q3D Extractor was used to extract the parasitic from the layout which were then used to calculate its impact on the converter design.

When utilizing a conventional power module and wide bandgap devices it becomes crucial to understand and simulate the capacitive couplings between the power module and the heatsink. The reason being that capacitive coupling introduce increased switching losses and EMI, which are crucial to address early in the design phase. The capacitive contribution of a power module was initial investigated for a 10 kV SiC power module. The purpose of the experiment was to validate the understanding of the capacitive network and to validate the use of finite element software. The capacitive network was selected for the 10 kV SiC power module due to the high dV/dt and low dI/dt introduced during switching transients. The simulation and measurements showed perfect agreement, validating the understanding of the system.

With the modelling approach validated, the next step was to develop the initial layout of the T-type converter and evaluate its performance. The layout was designed for the power module, gate driver and power routing PCB. During the design phase it was observed, that the gate driver circuits and required clearance introduced a substantial volume contribution. To reduce the volume of the gate driver circuit a novel bootstrap circuit for a T-type converter was proposed. To evaluate the performance obtained by the proposed bootstrap circuit, a new mathematical method was developed to calculate the modulation index limit. A new method was needed as the conventional method uses rule of thumb estimations, providing a rough estimate of the modulation index limit. Using the new mathematical model, the bootstrap circuit for the T-type converter was evaluated which showed a higher safe modulation index limit was obtained, compared to the conventional half bridge bootstrap supply. The proposed bootstrap circuit was not used in the prototype, due to the presence of a modulation index limit.

The new challenge when design a converter system, is the increased impact of parasitics from the layout. The research in the field has mainly been focused on the power module and the parasitic it introduces, however the surrounding components as the gate driver and power routing PCB also contributions with parasitics, impacting the switching performance of the power module thus a bigger picture is needed for overall performance improvement. Another layer of complexity is added when evaluating a T-type converter, as it introduces two power loops which should be optimized for a low inductance, compared to a half bridge which only introduces a single power loop. The power loop of the T-type converter encloses three semiconductor unavoidable increasing the power loop inductance, compared to a half bridge converter.

The performance of the power module, gate driver and power routing PCB were simulated in LTspice using the layout parasitics extracted from ANSYS Q3D Extractor, semiconductor models from the manufacturer and models of passive components obtained from LCR measurements. Based on the evaluation of the switching performance of the power module, a RC DC-link snubber was placed inside the power

module. The capacitance provides a low impedance path for the switching current, circumventing the inductance contribution from the power module terminals and thereby reducing the voltage overshoot across the switches. The resistor dampens the oscillation between the external DC-link and the DC-link snubber inside the power module, reducing voltage overshoot and generated EMI. The performance of the layout was experimentally validated, showing good agreement on the switching period time scale. A minor discrepancy between the measured and simulated turn on dV/dt was observed, where a mismatch in measured and simulated IV-characteristics were identified as root cause of deviation. In general the power module performed as simulated, and a three phase setup is build based on the design.

The purpose of performing experimental test with the three phase system was to validate the converter design, the system modelling and ensure continuous stable operation. To validate stable operation the three phase T-type converter was operated with a DC-link voltage of 560V, an output current of 10 A rms and a switching frequency of 64 kHz. By measuring the output voltage of the power module, clean switching was confirmed during a full fundamental period. Furthermore only small temperature increases of the heatsink and filter was observed. The current ripple through the filter inductor was measured and compared with simulation. The measured and simulated current ripple showed perfect agreement, validating the modelling approach taken when considering the converter system. The output current harmonics was measured, showing low magnitudes of switching harmonics, validating a sinusoidal output with only $60cm^3$ of output filter per phase. The small volume of the output filter in combination with the converter operation validates the frequency limit provided by the Pareto Algorithm at 70 kHz. Only a minor reduction in filter size would be obtained by increasing the switching frequency or level of topology with the penalty of increase cost, heatsink or gate driver volume. The validation of three phase converter concludes the design process presented in this thesis, which covers the initial objective selection of a design topology and switching frequency and the modelling complexity needed for local and system simulations with experimental validation.

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Papers

Appendix A

Cost, Efficiency and Power Density Pareto Investigation of Three Phase Inverters.

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Cost, Efficiency and Power Density Pareto Investigation of Three Phase Inverters.

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Keywords

Wide bandgap devices, Efficiency, High power density systems, Converter circuit, Three-phase system.

Abstract

Wide bandgap devices are enabling an increase in the efficiency and power density of converter systems. The properties of the wide bandgap devices are changing the optimum design parameters for converters. With a growing diversity of wide bandgap devices, it becomes increasingly difficult to select the optimum components, topology and design parameters for an application. This paper adresses challenges in identifying the optimum topology for wide bandgap devices and which components to select. Based on commercially available products and analytic equations, an algorithm is developed to aid the topology investigation. A three-dimensional plot is extracted from the algorithm, evaluating cost, efficiency and power density. The designs visually presented are the circuit combination fulfilling the design constraint. The algorithm allows the designer to select a topology, switching frequency and components based on an objective comparison.

Introduction

The emergent of wide bandgap (WBG) semiconductor devices and their improving readiness level are leading towards a paradigm shift within the field of power electronics [1]. Wideband gap devices such as gallium nitride (GaN) and silicon car-

bide (SiC) power component demonstrates superior performance in regards to low switching losses and for SiC high voltage withstand capability, compared to its silicon counterparts [2]. Utilizing wide bandgap semiconductors new power conversion products can increase efficiency and significantly reduce system size [3]. The new wide bandgap devices results in a shift of the optimum converter design for a given application. Failing to evaluate and accurately compare converter topologies and design variables might yield a converter, which is more expensive, physically larger and less efficient than its alternatives. A multi objective optimization algorithm named Pareto, is utilized in this paper to investigate the optimum three-phase inverter topology when implementing the new WBG devices. Pareto optimization have, for example, been used for local power density and effeciency optimization of inductors [4]. Due to the interactions between converter components, determning the switching frequency based on a local optimization of a component does not guarantee the convergence to a system optimum. Limited literature is available for complete converter systems. A Pareto front showing the outline of the optimum converter solutions is published for a single phase inverter in [5], the Pareto plot evaluates efficiency and power density omitting cost in the comparison. This paper present an algorithm, where a three-dimensional Pareto plot is extracted. The three-dimensional plot quantifies efficiency, power density and cost for a three phase inverter, excluding the external load. The Pareto algorithm is developed based on analytical equations and commercially available products, allowing for fast computation.

Pareto Plot for a three phase inverter

The Pareto algorithm utilized for the topology investigation is a multi objective optimization algorithm, the optimization objectives are cost, effeciency and power density. The topologies under investigation are the two-level, T-type, active NPC (ANPC) and Pi-type converter shown in Fig. A.1. The inverter includes a LC output filter which are proposed for AC drives to supress common mode (CM) and differential mode (DM) $\mathrm{d}u/\mathrm{d}t$ [6].

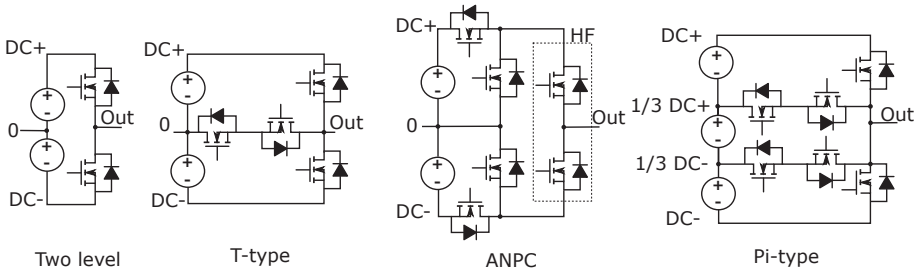

Figure A.1: Illustration of the topologies investigated in the study, HF refers to the leg being operated with a high switching frequency

The single phase two level converter shown in Fig. A.1, consist of a halfbridge.

The topology can output either DC+ or DC−. The two level converter is the most commonly used topology in the low to medium voltage range, due to the control simplicity and low cost. The T-type topology shown in Fig. A.1 can output DC−, 0 and DC+, enabling three output voltage levels. The additional output voltage level reduces the switching voltage to half the DC-link, significantly reducing the energy dissipated during switching. The top and bottom switch are blocking the full DC-link voltage, were as the middle leg switches are blocking half the DC-link voltage. In the T-type all four switches are operated with high switching frequency, distributing the power dissipation between all dies, during a fundamental output cycle. The ANPC shown in Fig. A.1 has three output voltage levels, similar as the T-type. The half bridge with the midpoint being the output terminal, is operated at high frequency. The four switches connected to the DC-link is switched dependent on the fundamental output cycle, and is mainly contributing with conduction losses. The power dissipation is as a consequence mainly located in the high frequency half bridge. The Pi-type shown in Fig. A.1 is based on the circuit of the T-type. The Pi-type converter has four output voltage levels, DC+, $\frac{1}{3}$DC+, $\frac{1}{3}$DC− and DC−. Four output voltages levels enables smaller passive components. The power dissipation will be distributed between all dies, during a fundamental output cycle. The blocking voltage of the middle legs should as a consequence be $\frac{2}{3}$ of the DC-link voltage. Bottom and top switch are blocking the full DC-link voltage, as was the case with the T-type topology.

Each topology presented in Fig. A.1, is separated into the major components sketched in Fig. A.2. A cost, volume and power loss function is associated with each

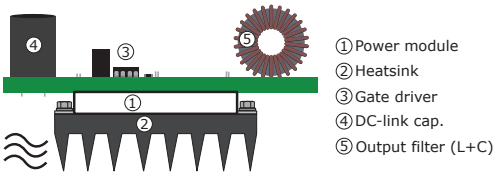

Figure A.2: Illustration of the major components in an inverter. The components shown are accounted for in the Pareto plot.

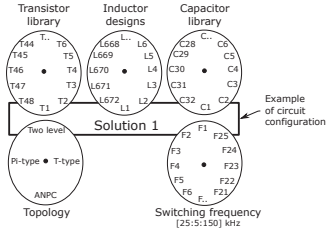

Figure A.3: Graphical illustration of the libraries creating a large solution space of circuit configurations

component presented in Fig. A.2. The impact on the objectives vary depending on the component. Each component has an extensive datasheet library and several design parameters which are creating a large number of circuit configurations for all topologies at each switching frequency. A graphical illustration of the potential circuit configurations are displayed in Fig. A.3. In this paper, the focus will be on the modelling of selected components with a major influence on the results presented in the Pareto plot. The models which will be presented are the power loss of a two level power module, output inductor and the volume of the heatsink.

Power module

The semiconductor power losses are calculated based on their stored capacitive energy in the output capacitance [7]. The capacitive power dissipation is caused by discharging the output capacitance of the switching semiconductor and charging the connected parasitic capacitances. Due to the complexity related to calculating the charging efficiency of a voltage dependent capacitance, a 50% charging effeciency is assummed. A charging efficiency of 50% is true for a resistive charging of a constant capacitance [8]. Using the simplification, the switching energy can be described as the capacitive contributions in (A.1) and (A.2) for a two level topology.

$$E_{oss(dis)} = \int_{U_{DC}}^{0} C_{oss}(u) \cdot u \, \mathrm{d}u \tag{A.1}$$

$$E_{oss(charge)} = \int_{0}^{U_{DC}} C_{oss}(u) \cdot u \, \mathrm{d}u \tag{A.2}$$

The evaluation of capacitive losses depends on the topology. For example the T-type discharging voltage in (A.1) will reduce from U_{DC} to $\frac{1}{2}\mathrm{U}_{DC}$ and (A.2) will be divided into two equations. One where the bottom leg is charged from $\frac{1}{2}\mathrm{U}_{DC}$ to U_{DC} and the middle leg from 0 to $\frac{1}{2}\mathrm{U}_{DC}$. Parameters such as capacitance, on-state resistance and price of the semiconductors are specified in a library. The library contains GaN transistors, silicon (Si) and SiC MOSFETs from several manufactures, with on-state resistances ranging from 17mΩ to 120mΩ. When calculating the conduction losses, the junction temperature is taken into consideration by implementing a linear interpolation between the two on-state resistance provided in the datasheet. The conduction and switching losses are then calculated at each frequency, selecting the switch combination providing the lowest combined losses. An example of switch loss calculation is presented in (A.3) for a three phase, two level topology.

$$P_{SW} = 3 \cdot \left(I_{rms}^2 \cdot R_{DS(on)}(T_j) + 2 \cdot \sum E_{oss} \cdot f_{sw} \right) \tag{A.3}$$

The estimated power loss does not take into consideration the potential soft switching occurring, as an effect of deadtime and output current. The switch losses are provided as inputs for the heatsink to estimate the required volume for cooling.

Output inductor

The Pareto algorithm creates inductor designs by sweeping a variety of design variables. The design variables are wire thickness (AWG), number of wires in parallel and a library of cores. Each inductor consists of a single layer of windings. A single layer is selected to obtain a low equiavalent parallel capacitance of the inductor. The number of turns are limited by core saturation and physical core dimensions. The inductance obtained for each inductor design is calculated and used for determining

the current ripple. The equation for calculating the peak to peak ripple is presented in (A.4). [9]

$$\Delta I = \frac{1}{8} \cdot \frac{U_{DC}}{f_{sw} \cdot L_f \cdot (n_{level} - 1)} \tag{A.4}$$

The current ripple can then be utilized for calculating the magnetic field. The magnetic field is used in an empirical flux density equation specified from the manufacture [10]. The empirical equation is presented in (A.5).

$$B_{ripple(max)} = \left(\frac{a + b \cdot H_{ripple(max)} + c \cdot (H_{ripple(max)})^2}{1 + d \cdot H_{ripple(max)} + e \cdot (H_{ripple(max)})^2} \right)^x \tag{A.5}$$

The average between the minimum and maximum flux density is used to calculate the power dissipation per unit volume as given in (A.6).

$$PL = a \cdot B_{pk}^b \cdot f^c \quad [mW/cm^3] \tag{A.6}$$

The power dissipation is calculated for the high and low frequency current ripple, utilizing the volume determined by the core dimensions. RMS current and current ripple is used to calculate the copper losses of the windings. The core and copper losses are summed up for the inductor and utilized for the Pareto plot.

Heatsink

The heatsink volume accounts for a significant volume contribution for hard switched topologies. It is necessary to introduce a penalty volume as an effect of the power dissipation. To avoid time consuming thermal FEM simulations, an assumption of an inversely proportional dependency between heatsink volume and thermal resistance is assumed. The equation utilized for calculating the heatsink volume is presented in (A.7).

$$Vol_{heatsink} = K_{heatsink} \cdot \left(\frac{P_{SW}}{T_j - T_{amb}} - \frac{R_{th(j-c)}}{n_{dies}} \right)^{-1} \tag{A.7}$$

P_{SW} is the switch power dissipation for three phases, T_j is the junction temperature, T_{amb} is the ambient temperature, $R_{th(j-c)}$ is the thermal resistance from junction to case, n_{dies} is the number of semiconductors dies dissipating power and $K_{heatsink}$ is the ratio between volume and thermal impedance for a heatsink $\frac{m^3 \cdot W}{K}$. The heatsink constant is calculated by utilizing the datasheet for a forced cooled heatsink.

Selection of design candidates

Based on input parameters as output current, output power, DC-link voltage and switching frequency a vast amount of circuit configurations are generated. The circuit configuration are initially reduced by constrains as maximum allowed current

ripple for output inductors, minimum required DC-link capacitance for protection and excessive power dissipations. An example of the excessive power dissipation, is if the power dissipation of the semiconductors are causing the requirement of a negative thermal impedance for the heatsink. The value becomes negative due to excessive cooling requirements and the design is removed by a selection routine. Sweeping the circuit configurations over a wide switching frequency results in millions of potential configurations. The selection routines reduces the solutions space from millions to thousands of circuit configuration candidates. The thousands of design candidates are extracted and represented in a 3-dimensional plot, with each dimension representing one of the optimization objectives. What is known as the Pareto optimum is exceeded when none of the objectives are improving. Relating to converter design, the Pareto optimum will be surpassed when the switching frequency obtains a value where the filter volume is no longer reduced beyond the heatsink volume increase and the combined power dissipation is increased.

Pareto front of the results

The thousands of circuit configurations can be seen in the three-dimensional Pareto in Fig. A.4 with a frequency sweep from 25 kHz to 150 kHz. The large diversity of solutions in Fig. A.4, presents the importance of selecting the optimum switching frequency and components to use. Failing to do so, can provide a significantly more expensive solution with lower performance.

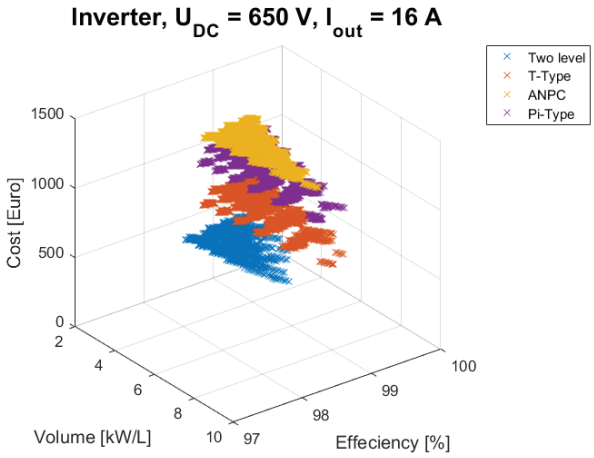

Figure A.4: Three-dimensional Pareto plot of a 7.5 kW three phase inverter with DC-link, heatsink and output filter.

In Fig. A.5 the cost and efficiency is presented in a two dimensional plot. If comparing the cost of the ANPC and T-Type, a price difference of approximately 300,- Euro is identified. At a specific switching frequency, the passive components

are of equal values and cost. A difference in power dissipation and thereby heatsink size and cost might be observed, however the price of aluminium is small, compared to the full converter system cost. The cause of cost difference can as a consequence be isolated to the semiconductors and the gate driver circuitry needed. The hypothesis of the cost being heavily dependent on the number of the semiconductor dies can be validated from the results shown in Fig. A.5. The number of semiconductor devices per phase increases from two switches of the Two level topology to four for the T-type and six for both ANPC and Pi-type. By studying the cost in Fig. A.5 significant price differences can be observed and correlated to the number of dies used in the topology. The price reduction from three level ANPC to the four level Pi-Type can be explained by the reduced size of the output filter passives.

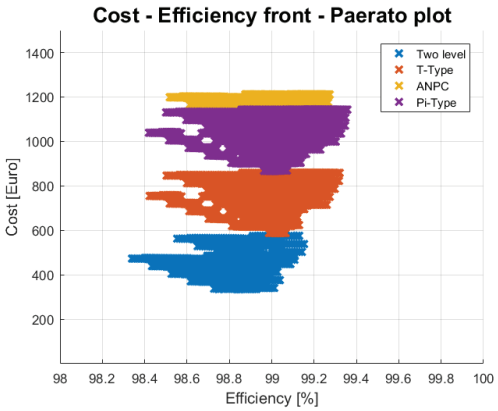

Figure A.5: Two dimensional Pareto plot, showing cost and efficiency for a 7.5 kW three phase inverter with DC-link, output filter and heatsink.

In Fig. A.6 a two dimensional outline of the optimum circuit configurations are presented by ignoring cost as an optimization objective. The outline is open towards lower power densities, due to the limited frequency range investigated. It implies that circuit configuration below 4 kW/l exist, but are not investigated due to the low power density achieved.

From Fig. A.6, it can be seen that a high power density is achieved by the T-type and Pi-type topology.

A reason for why the T-type achieves a higher power density than the ANPC is due to the distribution of its power dissipation between several dies. The Pi-type does not obtain a large power density compared to the T-type due to additional volume required by the power module, gate driver circuitry and DC-link, outweighing the filter and heatsink volume reduction. What is not evident from the Figure A.6 is the effect of the switching frequency. The plot start at a frequency of 25 kHz, at this frequency most solutions yields a low power density and a high efficiency. As the switching frequency increases, the filter volume and the efficiency decrease, the solutions then travels from highest efficiency to highest power densities. Around 75 kHz their maximum

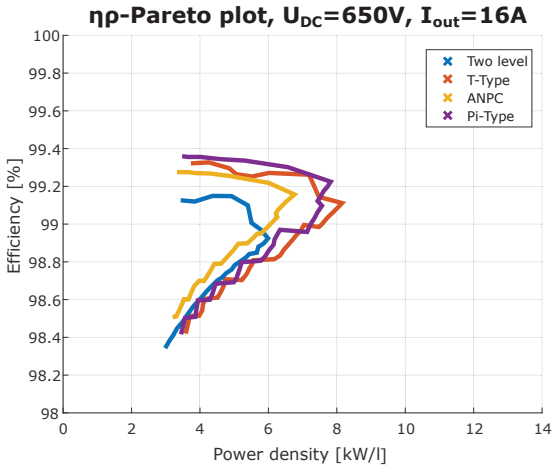

Figure A.6: Pareto front of power density and efficiency for an 7.5 kW three phase inverter with DC-link, output filter and heatsink.

power density is achieved, meaning increasing the switching frequency will not yield a significant filter volume reduction compared to the heatsink volume increase. For switching frequencies above 75 kHz the Pareto optimum has been surpassed, meaning all solutions of higher frequencies will obtain a lower efficiency and power density. A T-type back-to-back converter utilizing a switching frequency of 48 kHz is reported in literature to obtain comparable efficiency and power density [11]. The back-to-back Si/SiC converter was reported to have an efficiency of 96.5 % and a power density of 2.9 kW/L. If assumed identical efficiency of rectifier and inverter, an efficiency of 98.2% and power density of 5.8 kW/L was achieved. The power density and efficiency are comparable to what is obtained in the Pareto plot, when also taking into consideration the addition of an EMI filter on the input.

Comparison of topologies

The multilevel topologies achieve relatively small increases in power density and efficiency compared to the two-level topology. The two-level being a simple and cheap topology coincides with the fact that alternative topologies are rarely found in industrial products. In applications where efficiency and power density are prioritized compared to manufacturing cost would yield a potential market for other topologies. Comparing an ANPC to a T-type, the system volume and cost of the ANPC is increased due to the additional transistors and gate circuitry required, making the T-type a cheaper topology achieving comparable efficiencies and power densities. The four level Pi-type converter achieves the highest efficiency. If the Pi-type converter is selected, one should bare in mind the additional complexity introduced in regards to manufacturing and control, which are not quantified in the Pareto plot. With a goal of

increased efficiency and power density the T-type converter therefore presents itself as the optimum topology due to the addition of only two switches. The T-type achieves high efficiency and power density with the lowest cost increase, when comparing it to its multilevel alternatives.

Discussion of assumptions

The Pareto relies on a number of inputs, assumptions and designs constraint. The analytical equations are valid, if its set of assumptions are correct. In the Pareto plot, the switching losses are assumed to be dominated by the loss contribution associated with charging and discharging output capacitances of semiconductors. The switching loss being contributed by only the capacitances are an optimistic assumption. Due to the gate resistance and gate-drain capacitance, the switching transient will not occur instantaneously. Resulting in a switching loss contribution associated with the output current. An increase in the switching losses will penalize all converter topologies in the Pareto plot. Firstly the balance between optimum R_{DS} and E_{SW} will change, favouring the dies with lower E_{SW}. A decrease in the optimum switching frequency of the topologies are expected. The decrease in frequency is caused by the increase in heatsink volume penalty, when increasing the switching frequency. The filter inductance and size will as a consequence increase, lowering the power density for all topologies. The absolute values of efficiency, power density and cost will as a consequence be changed. All calculations for the topologies are performed based on the same assumptions, making it likely that only small relative variations between topologies will occur. The general conclusion regarding the relative performance of topologies will as a consequence not change. A test using the Pareto script is performed, validating the relative conclusion being unchanged. The test is performed by varying an amplification of the switching losses. The results shows a decrease of absolute efficiency and power density for all topologies, with small relative changes. Insignificant price variations were observed due to the selection of alternative dies and changing price of passive. The absolute variations in price for the topologies are neglectable, due to the cost currently being dominated by the number of wide bandgap devices and gate driver circuitry used.

Conclusion

The presented algorithm and Pareto plot quantifies the volume, efficiency and cost for multiple topologies. The Pareto front has been compared to existing designs, showing comparable efficiencies and power densities achieved in practise. The Pareto plot provides an approach of reducing the number of circuit configurations and selecting a design optimum with WBG and Si devices. Based on the inverter topologies investigated for motor drives with sinusoidal output, increasing the output voltage levels or choosing a more complex topology than a T-type will not yield a higher power density and only produce an insignificant efficiency increase with a significant cost increase.

The Pareto optimum limits the switching frequency for all topologies to a maximum of 75 kHz. Switching frequency above 75 kHz will result in a lower efficiency and a larger volume of the inverter.

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Appendix B

Common Mode Current Mitigation for Medium Voltage Half Bridge SiC Modules

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Keywords

Wide bandgap devices, Silicon Carbide (SiC), EMC/EMI, Noise, New switching devices.

Abstract

Medium voltage 10 kV Silicon Carbide MOSFETs, introduce challenges regarding converter design. Very high rate of voltage change and capacitive couplings to for example cooling systems cause increased electromagnetic interference. The aim of this paper is to accurately model the capacitive coupling to a heat sink and experimentally validate the model. An analytic model of the heat sink is developed which is demonstrated to be in excellent agreement with experimental results. The experimental result validates the modelled heat sink network allowing engineers to choose a suitable grounding impedance to comply with the electromagnetic compatibility regulations.

Introduction

The emergent wide-band gap semiconductor devices, such as Silicon Carbide (SiC) MOSFETs introduce new opportunities for converter designers. Key advantages of SiC MOSFET are their low switching losses and medium voltage withstand capability [1]-[3]. The low switching losses at medium voltage are obtained by achieving very fast switching. The focus of this paper is on the rate of change in voltage (dv/dt), which typically may reach 30 kV/μs [4]. This is an order of magnitude larger compared to Si IGBT. The combination of parasitic capacitancens, high dv/dt and grounding the

heat sink introduces some challenges when building a medium voltage SiC converter in practice [7],[8]. The effect of the device and module parasitic capacitive coupling is therefore crucial to understand if the common mode currents need to be addressed to obtain reliable operation and compliance with the electromagnetic compatibility (EMC) regulations. Common mode currents are desired to be attenuated to prevent excessive stress on components and maintaining fidelity of control signals. Failing to do so early in the design phase could result in a need to reduce the dv/dt and as a consequence also reduce switching frequency and power rating of the converter. The half bridge parasitics are key parameters in the design phase to calculate the magnitude of common mode currents. The aim of this work is to address and analyse it. A double pulse test setup was built with the purpose of experimentally validating an impedance network model of the heat sink.

Experimental and model details

The double pulse test setup and its schematic are shown in Fig B.1.

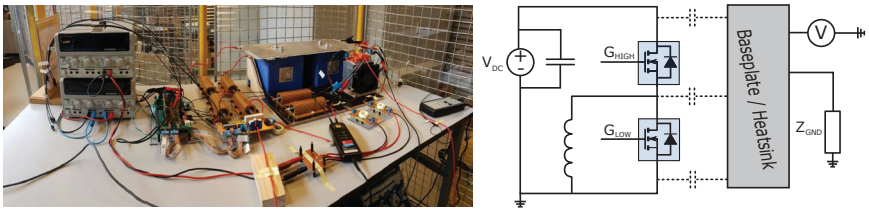

Figure B.1: Double pulse setup with half bridge module and grounded heat sink

The problem identification performed in this paper is focusing on a half bridge module with first generation 10 kV SiC MOSFETs and SiC JBS diodes. The specific half bridge module used is shown in Fig. B.2 and was custom packaged at the Department of Energy Technology, Aalborg University. The parasitic capacitances of the

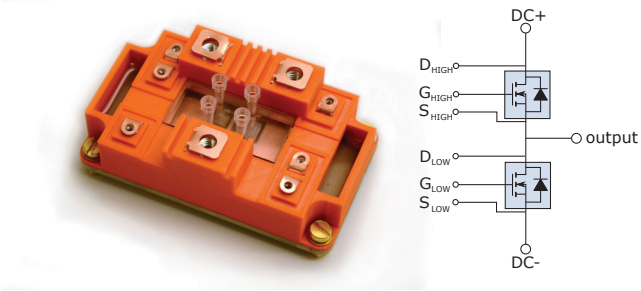

Figure B.2: Image and schematic of the half bridge power module consisting of 10 kV SiC MOSFETs and external SiC JBS diodes

module is listed in Table B.1. According to ANSYS Q3D, a capacitive coupling of

149 pF is present between the output of the half bridge module and the heat sink due to the layout and thickness of direct bonded copper (DBC) substrate.

A gate driver is required to drive the half bridge power module. A gate driver with low isolation capacitance of the isolating transformer was therefore developed for the experimental setup [5]. The gate driver is shown in Fig. B.3.

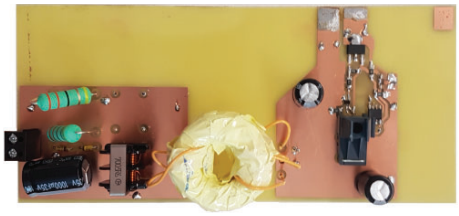

Figure B.3: Gate driver with active Miller clamping circuit for medium voltage SiC MOSFET

The isolation transformer has a coupling capacitance from primary to secondary of only 2.6 pF, attenuating the common mode currents flowing through the isolation boundary [6], ensuring fidelity in control signals. The capacitive coupling of the gate driver is neglected in this work due to its insignificant impact on achieving an accurate parasitic network representation of the heat sink.

Modelling of heat sink

With a given dv/dt the impact of external capacitive couplings on control signal fidelity and EMI is quantitatively analyzed. The parasitic network of the heat sink is displayed in Fig. B.4 with values of parasitics presented in Table B.1. The stray inductance of the power module is not included in the analysis due to the relative low rate of current change and value of inductances contributing with a negligible voltage oscillation in the midpoint voltage compared to the medium voltage switching transient. The module parasitics were numerically simulated and extracted in [9] utilizing ANSYS Q3D on the module design. The simulated values were supplemented by external parasitics, obtained by measuring the impedance of the surrounding components using a Keysight E4990A impedance analyser.

A floating heat sink minimizes the current transfer from output to heat sink. The current returns as common mode current through the DC+ and DC- plane of the module. The DC+ and DC- common mode currents find their return path predominantly through the MOSFET's drain-source capacitance and the DC-link capacitor. The floating potential of the heat sink works as a medium voltage antenna and is a source of radiated EMI. If the heat sink is shorted to ground it is equivalent to inserting a snubber capacitance in parallel to the MOSFET's containing parasitic stray inductance as an effect of grounding the heat sink with a wire. The effect of shortening the heat sink to ground is an increase in inrush currents, and thereby an amplification of switching losses, and unintended high frequency current oscillation through the DC-link as

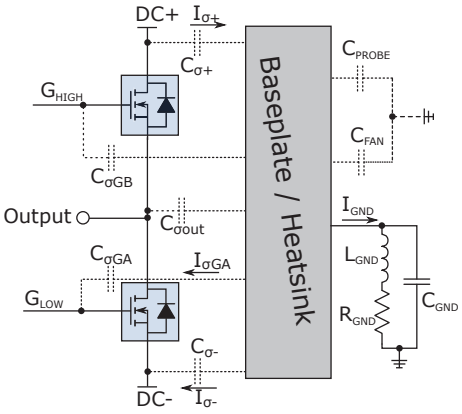

Figure B.4: Impedance network coupling the heat sink and half bridge power module

Table B.1: Parasitic parameter values for heat sink modelling

Parameter	Value	Determination
$C_{\sigma+}$	100.5 pF	ANSYS Q3D
$C_{\sigma GB}$	21.6 pF	...
$C_{\sigma out}$	149 pF	...
$C_{\sigma GA}$	18.7 pF	...
$C_{\sigma-}$	45 pF	...
C_{PROBE}	8 pF	Impedance analyser
C_{FAN}	80 pF	...
R_{GND}	235 Ω	...
L_{GND}	25 μH	...
C_{GND}	50 pF	...

common mode currents and to the gate of the MOSFET's. The effects are caused by the undamped resonance circuit consisting of the parasitic capacitances and the inductance of the heat sink grounding. To quantify this two selected grounding impedances are simulated using LTspice. In one case a stray inductance of 500 nH (L_{GND}) and a resistance of 0.5 Ω (R_{GND}) is inserted when shortening the heat sink to ground, which emulates a piece of grounding wire. The effect of inserting an inductance with low resistance is a high frequency resonance circuit with low damping factor as shown in Fig. B.5. Allowing a parasitic high frequency resonant circuit is not desirable from an EMC or switching loss perspective. One solution is grounding the heat sink through a resistor, which dampens the oscillations. As an example a grounding impedance of 235 Ω is simulated as shown in Fig B.5. The results shows a decrease in switching loss and a resonant circuit with a large damping, dampening the current oscillations to the DC potentials and the gate driver. The subscript of the current are referring to Fig. B.4 representing the parasitic network. It is important to consider connected auxiliary equipment, such as a cooling fan and, the contribution to the parasitic network.

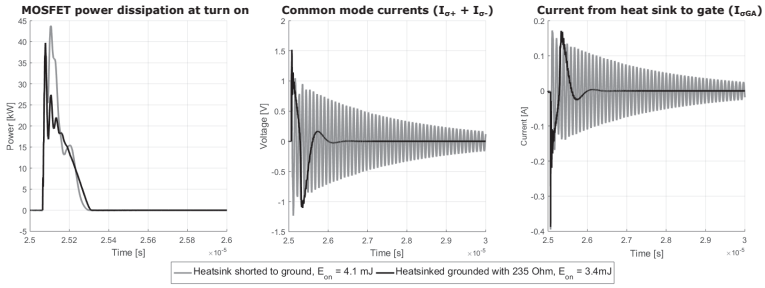

Figure B.5: Simulated effect of connecting the heat sink to ground with and without resistance

To choose a suitable grounding impedance, an analytical model has been developed based on Fig. B.4 circuit and experimentally validated. When developing a small signal model for the heat sink, some assumption are made. Since the signal of interest is in the MHz range, a 50 Hz voltage source supplying for example a cooling fan can be neglected in a small signal model. The impedances in Fig. B.4 are combined into three equivalent impedances based on their connections and signals that are desired as outputs. Equation (B.1) is the impedance of the floating point to heat sink. (B.2) is from heat sink to the fixed potentials as DC+, DC- and ground. (B.3) is the impedance of the grounding connection of the heat sink.

$$\frac{1}{Z_1(s)} = \frac{(C_{\sigma out} + C_{\sigma GB}) \cdot s}{R_{EQ} \cdot (C_{\sigma out} + C_{\sigma GB}) \cdot s + 1} \tag{B.1}$$

$$\frac{1}{Z_2(s)} = \frac{(C_{\sigma+} + C_{\sigma-} + C_{\sigma GA} + C_{PROBE} + C_{FAN}) \cdot s}{R_{EQ} \cdot (C_{\sigma+} + C_{\sigma-} + C_{\sigma GA} + C_{PROBE} + C_{FAN}) \cdot s + 1} \tag{B.2}$$

$$Z_{GND}(s) = \frac{\frac{1}{C_{GND}} \cdot s + \frac{R_{GND}}{L_{GND} \cdot C_{GND}}}{s^2 + \frac{R_{GND}}{L_{GND}} \cdot s + \frac{1}{L_{GND} \cdot C_{GND}}} \tag{B.3}$$

Including the equivalent series resistance (ESR) of DC-link, R_{ds-on} of MOSFET's, resistance of connections would drastically increase the complexity of the model with limited impact. The impact will be small because the dominant part of the damping is being contributed by the heat sink resistor. An equivalent resistance representing all the other parasitic resistors apart from the heat sink grounding, is therefore chosen to be R_{EQ} = 5 mΩ to neglect it in the simulation and allowing parallel connection of parasitic capacitances. With the simplifications implemented, the equations can be converted into a simple block diagram structure for the heat sink voltage and currents. The block diagram is given in Fig. B.6.

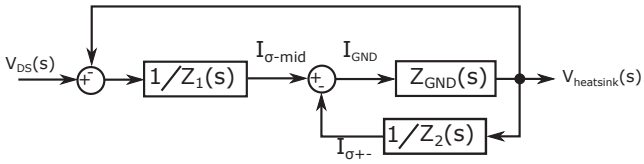

Figure B.6: Block diagram of the heat sink impedance network related to grounding (Z_{GND}) and power module (Z_1, Z_2).

$I_{\sigma-mid}$ is the current flowing through the DBC from the floating plane to the heat sink. The current $I_{\sigma+-}$ is the current conducted from the heat sink through the plane connected to DC+, DC−, C_{FAN} and C_{PROBE}, which is the common mode current flowing as an effect of the chosen grounding impedance. The I_{GND} is the current through the grounding impedance, usable for determining the power dissipation and choosing the ratings of the grounding impedance. The common mode current depends on the impedance network of the module, heat sink grounding as well as the dv/dt. The dv/dt should be limited due to the Miller current flowing through the gate-drain capacitance C_{GD}. Due to the very high dv/dt, a large Miller current will be flowing through a MOSFET during its off state as a result of switching the complementary transistor in the half bridge module. The Miller current causes a voltage rise, potentially causing a false turn on even though a negative gate bias is applied. The controlling factors for the highest allowable dv/dt are V_{GS-th}, C_{GD}, C_{GS}, R_{G-INT}, L_{G-INT}. In order to quantify this, the voltage rise is analysed using the model shown in Fig. B.7.

The method of calculating Miller current is well documented in [10] and [11]. The purpose of mentioning it in this paper is to determine a dv/dt which prevents false turn on when considering safety margins, device parameters and their dependencies. Equation (B.4) describes the relationship between the imposed Drain-Source voltage (V_{DS}) and the rise of the internal gate voltage (V_{GS-INT}). The equation is used to determine a maximum dv_{DS}/dt of 20 kV/μs when considering a safety margin for temperature dependency. The minimum value of external gate resistor is therefore

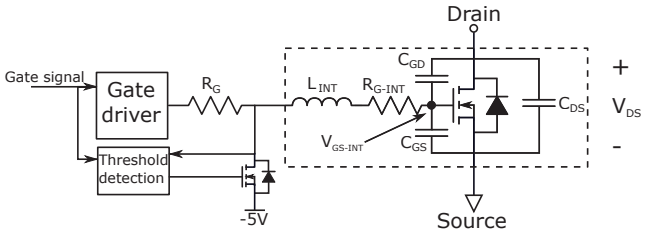

Figure B.7: Model of SiC MOSFET and gate driver circuit with active Miller clamp

chosen to comply with the upper limit of imposed $\mathrm{d}v_{DS}/\mathrm{d}t$.

$$\frac{V_{GS-INT}(s)}{V_{DS}(s)} = \frac{L_{INT}\cdot C_{GD}\cdot s^2 + C_{GD}\cdot(R_G + R_{G-INT})\cdot s}{1+(R_G+R_{G-INT})\cdot(C_{GD}+C_{GS})\cdot s + L_{INT}\cdot(C_{GD}+C_{GS})\cdot s^2} \quad \text{(B.4)}$$

The safety margin of the $\mathrm{d}v/\mathrm{d}t$ is imposed by the negative temperature coefficient of the threshold voltage. When the temperature increases, the threshold voltage decreases [12]. A clear requirement of a Miller clamp and negative gate bias for high dv/dt operation is identified by the simulation performed with (B.4).

Experimental results

In Fig. B.8 a test at a DC-link voltage of 5 kV is presented, comparing output voltage and heat sink voltage of the experimental results to the simulation results. The purpose of comparing is to evaluate on the correlation between simulation and experiment. The measurements are performed with a Teledyne Lecroy PPE 6 kV high voltage probe and a CP030 current probe. The probes have a bandwidth of 400 MHz and 50 MHz, respectively.

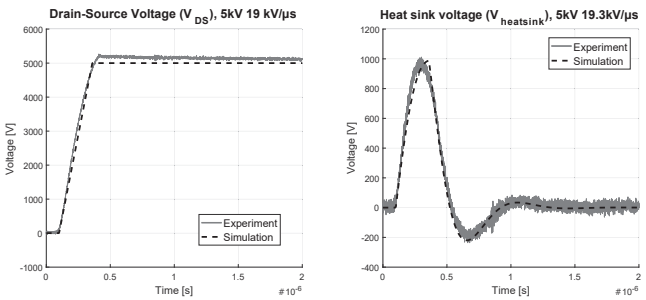

Figure B.8: Comparison between simulation and experiment results at 5 kV with 19 kV/μs.

Fig. B.8 shows a close correlation between measured heat sink voltage and the response simulated using the model in Fig. B.6. Excellent agreement is present in

regards to amplitude, damping and oscillation frequency. The damping introduced to the system is dominated by the grounding resistor, which is implemented by a LCR circuit matching its measured frequency response. To corroborate the validity of the model it was also tested at different voltages. As an example measurements at 3.5 kV are shown in Fig. B.9.

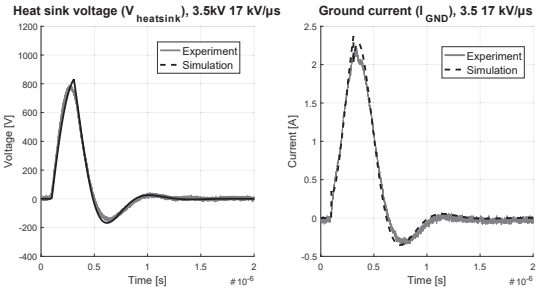

Figure B.9: Comparison between simulation and experimental results at 3.5 kV with 17 $kV/\mu s$.

General for the simulated current through the impedance network I_{GND} is a rapid increase at 0.1 μs and decrease at 0.3 μs which diverges from the experimental results by an offset. The deviation is a result of the circuit representation for the grounding impedance. The grounding impedance is represented by a resistor and an inductor in parallel with a capacitor. Better agreement can be obtained if a more detailed representation of the grounding impedance is chosen.

The time period of oscillation is significantly affected by the capacitor values connected to the heat sink. The sensitivity to changes in capacitance values is demonstrated by removing the 80 pF and 8 pF of coupling capacitance contributed by the fan and probe, respectively. The responses with and without auxiliary capacitances are shown in Fig. B.10.

Table B.2: Effect on heat sink voltage of an increase in capacitance with the subscript referring to the impedance transfer function

$$C_1 = C_{\sigma-} + C_{\sigma GA}$$
$$C_2 = C_{\sigma+} + C_{\sigma-} + C_{\sigma GA} + C_{PROBE} + C_{FAN}$$

Parameter	Amplitude	Period
$C_1 \uparrow$	$\uparrow$	$\uparrow$
$C_2 \uparrow$	$\downarrow$	$\uparrow$

By comparing the response in Fig. B.10 it is clearly visible that omitting the fan and probe capacitances decreases the time period of the ringing and increases the amplitude, causing the simulation result to deviate from the measured response. The parameter sensitivity of the response verifies a high accuracy of the modelled

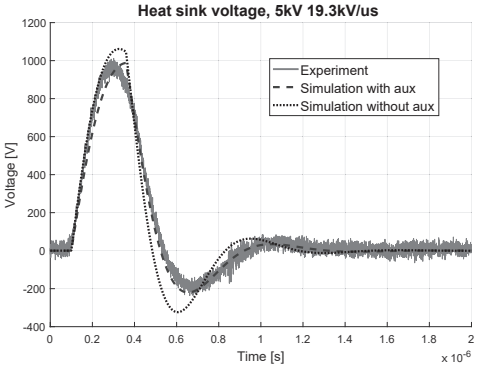

Figure B.10: The effect of omitting the auxiliary connected capacitances contributed by the fan and voltage probe.

impedance network for the heat sink. Combined with the excellent agreement between experimental results and impedance network in amplitude, frequency and dampening at all voltage levels tested, the usefulness of the model is validated. It demonstrates clearly the ability to determine the common mode currents flowing through the heat sink to the DC-link, the ground current and the effect on the gate driver circuit.

With the model accuracy validated the impedance network can be used to explore the effects of a parasitic capacitance increase on the heat sink voltage. The qualitative relationships are given in Table B.2. The reduction of C_2 will reduce the ringing period and diminish the duration of noise. The penalty of reducing the capacitance will be an increase in heat sink voltage. A reduction of C_1 and C_2 will significantly reduce the ringing period and may also reduce the amplitude, depending on the relative distribution of their capacitance values.

Revised power module design

A new power module design with reduced capacitive couplings was developed [9] and experimentally tested. To reduce coupling capacitances, the area of the copper planes are reduced, with special focus on minimizing the area of the output plane, while monitoring the penalty in stray inductance and resistance introduced. The modification details in [9] are performed to the extend that manufacturing and parasitic penalties are at an acceptable level. The parasitics of the revised module are given in Table B.3. The revised module contains a never generation of SiC MOSFET dies, resulting in different dv/dt. The revised module was tested in a similar manner as in Fig. B.1 and the heat sink voltage measured at 5 kV is presented in Fig. B.11.

As can be seen in Fig. B.11 good agreement is observed between measurement and simulation. Because of the reduction of the capacitance, the ringing period is reduced from 777 ns to 605 ns. The voltage amplitude is also reduced from 1000 V to 685 V with a grounding resistance of 276 Ω (R_{GND}), which is higher compared to the previous experiment. The duration and magnitude of the heat sink voltage

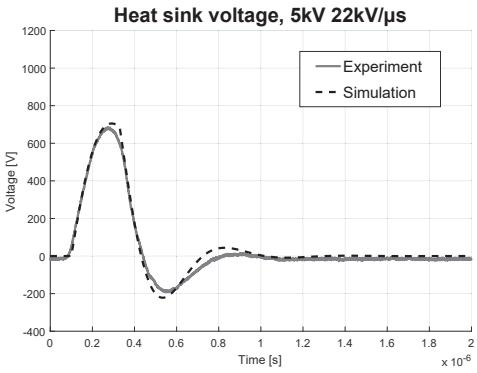

Figure B.11: Experimental test of the new generation of power module with reduced coupling capacitances to the baseplate.

Table B.3: Parasitic parameter values for the new generation of power module.

Parameter	Value	Determination
$C_{\sigma+}$	63.3 pF	Ansys Q3D
$C_{\sigma GB}$	11 pF	...
$C_{\sigma out}$	74.5 pF	...
$C_{\sigma GA}$	33.4 pF	...
$C_{\sigma-}$	33.4 pF	...
C_{PROBE}	8 pF	Impedance analyser
$C_{FAN-spaced}$	2.6 pF	...
R_{GND}	276 Ω	...
L_{GND}	25 μH	...
C_{GND}	50 pF	...

oscillation is therefore effectively attenuated by reduced parasitic capacitances in the revised module design.

The validation of Table B.2 and the heat sink model enables an experimental determination of the combined capacitance for (B.1) and (B.2) respectively by fitting the response of the heat sink voltage. The experimental determination of the parasitic coupling capacitances will only provide the capacitance sum (C_1 and C_2), thus some detail is not obtained. But the experimental determination of the coupling capacitance provides an alternative to a finite element method (FEM) software. An experimental determination will also include the auxiliary equipment which might be unknown prior to the construction of an initial prototype, and which may not be included in the software. It can also help, to identify parasitic effects of auxiliary equipment.

A double pulse test with a power module attached to a heat sink can then be used to determine switching losses and the capacitive coupling. The measurement requires a grounding impedance and an additional voltage probe. By using the experimentally obtained information an accurate impedance model of the ground currents introduced by the heat sink can be developed.

Conclusion

The modelled heat sink voltage and current response shows excellent agreement with the experimental measurements, validating the presented understanding of the parasitic heat sink network. The impedance network can be used to accurately model the conducted EMI produced by the parasitic couplings to the heat sink. It also allows the designer to identify critical parameters and to choose a grounding impedance, that is beneficial in achieving compliance with EMC regulations. A preliminary double pulse test of a power module can be utilized to experimentally obtain an impedance network omitting the need of a finite element method simulation.

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Appendix C

Modulation limit of bootstrap power supply circuits: case study of a three level T-type converter

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The layout has been revised.

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Keywords

Converter circuit, High power density systems, Pulse Width Modulation (PWM), Modelling, DC power supply.

Abstract

A bootstrap power supply is used to reduce the number of DC/DC converters needed for supplying the gate drivers. The advantage of a bootstrap is the reduction of size and cost for gate driver circuitry. The disadvantages is a modulation index limit. A modulation index limit can be compensated for, by increasing the DC-link voltage and thereby raising switching losses. It is therefore critical to accurately determine the modulation index limit, to prevent excessive losses, obtain safe operation and to evaluate the applicability of a bootstrap. The design rules of a bootstrap currently relies on rules of thumb estimations, generally underestimating the modulation index limit. In this paper a new generic method for calculating the modulation index limit is presented. The method takes on-state resistance, switching states and output current into consideration. The method is validated based on a proposed bootstrap circuit for a three level T-type converter. The proposed circuit achieves equivalent charging states as a half bridge bootstrap.

Introduction

A bootstrap circuit is a well known supply circuit for powering the high side gate driver in a half bridge converter. The advantage of utilizing a bootstrap is the reduction of DC/DC converters from four to one, in a three phase half bridge converter. Removing DC/DC converters decreases the size and cost of the gate driver circuits [1]-[3]. A disadvantages of using a bootstrap is the continuous switching required to ensure a stable gate driver voltage. In practice, the continuous switching requirement limits the modulation index and the usefulness of different modulation methods. Operating with a high modulation index is desired to decrease the DC-link voltage and

thereby reduce switching losses. If the modulation index limit is overestimated, the decreased supply gate voltage can cause thermal runaway of a switch or triggering of the under voltage lockout protection [4]. Identifying the modulation index limits is therefore essential to reduce switch losses and evaluating the bootstrap circuits potential in the specific application. The design and identification of the bootstrap circuit currently relies on rule of thumb estimations [5]-[7] and, as a consequence, does not provide a precise modulation index limit. The rule of thumb estimations are generally significantly underestimating the modulation index limit, increasing the switching losses of the converter. The reason why the commonly used method often is underestimating the modulation index limit, is due to the charging time is associated solely with the time constant of the bootstrap circuit. The minimum charging time is typically selected between 2.3 - 5 times the boostrap RC time constant, ensuring the bootstrap voltage is charged from 0% to above 90% of the final voltage [5]-[8]. These methods do not take into consideration the current dependent charging voltage or the minimum required voltage of the bootstrap circuit. Not considering the impact of the different voltages can cause substantial under or overestimation of the modulation index limit, with a critical impact on the converter performance. In this paper we present an extended general approach to accurately calculate the modulation index limit considering the current dependency of the charging voltage and minimum voltage requirements of the bootstrap. Considering charging voltage and minimum supply voltage allows the designer to evaluate the applicability of a bootstrap circuit for the given topology and semiconductor, and to select a suitable modulation index limit. The mathematical approach is verified numerically using a Spice simulator including semiconductor models.

Mathematical analysis of bootstrap

A typical bootstrap circuit contains a diode, resistor and capacitor as shown in figure C.1. During conduction of the lower switch Q_L, the bootstrap diode will be forward biased, charging the bootstrap capacitor C_{boot}, as is shown in figure C.2. The capacitor is charged through a current limiting resistor R_{boot}. The disadvantage of the bootstrap can be identified from figure C.3 and table C.1. During the conduction of switch Q_H, the diode is blocking and the bootstrap capacitor C_{boot} is not charged. If switch Q_H is kept on, the leakage and quiescent current of the gate driver circuit will discharge the bootstrap capacitor below the minimum required bootstrap voltage.

A key step in designing a bootstrap circuit is the selection of the bootstrap capacitor C_{boot} value. The bootstrap capacitance is selected based on the desired voltage drop, during a switching period. The minimum capacitance value can be obtained using equation (C.1). Q_g is the gate charge of switch Q_H, $I_{supply+lkg}$ is the leakage and quiescent current of the gate driver, f_{sw} is the switching frequency and ΔV is the maximum allowed voltage drop.

$$C_{boot(min)} = \frac{2 \cdot Q_g + \frac{I_{supply+lkg}}{f_s w}}{\Delta V} = \frac{2 \cdot Q_g + \frac{I_{supply+lkg}}{f_{sw}}}{V_{cc} - V_f - V_{min}} \tag{C.1}$$

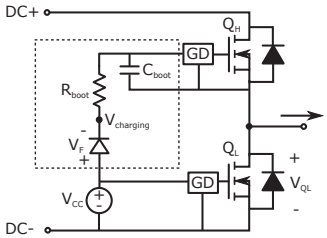

Figure C.1: Traditional implementatoin of bootstrap, connected to DC-.

Table C.1: Switching states of a halfbridge.

Q_L	Q_H	Effect on C_{boot}
Off	Off	Charging if $I_{out} > 0$ Discharging if $I_{out} < 0$
On	Off	Charging
Off	On	Discharging

The capacitance is in practice selected multiple times higher than the minimum value calculated in equation (C.1), to ensure a safe operation [9]. The next step of the design process is then typically to select a boot resistance R_{boot} based on the minimum on time of switch Q_L.

As a case study the bootstrap resistance is calculated in equation (C.2), using a capacitance of 1μF and a $t_{Low(on)}$ of 4μs.

$$R_{boot} = \frac{t_{Low(on)}}{4 \cdot C_{boot}} = \frac{4\mu s}{4 \cdot 1\mu F} = 1\Omega \tag{C.2}$$

The calculation here relies on a rule of thumb relationship between the time constant of the RC bootstrap circuit and the minimum on time [8]. A factor of four ensures the bootstrap voltage reaches within 2% of its steady state value. Equation (C.2) does not take the minimum safe bootstrap voltage and the charging voltage into consideration. An alternative method is therefore proposed in this paper, to obtain an accurate estimate of the modulation index limit.

Equivalent to the traditional method, the bootstrap capacitor sizing is initially determined based on a desired supply voltage ripple during a switching period. The sizing of the bootstrap capacitor is therefore performed utilizing the same equation as shown in equation (C.1). Instead of calculating the bootstrap resistance based on a desired minimum on time, the charging voltage is carefully considered, using Kirchoff's voltage law on the circuit in figure C.2 and C.3.

The charging voltage of the bootstrap is shown in equation (C.3), derived from figure C.2. Where V_{cc} is the voltage output of the DC/DC converter, V_F is the forward voltage drop of the bootstrap diode and V_{QL} is the voltage drop across the lower switch [5]. As the bootstrap charging current is small, the dominant voltage drop across the diode is the threshold voltage. Likewise since the charging current is small compared to the output current, the impact on the voltage drop across switch Q_L is neglectable.

$$V_{charging} = V_{cc} - V_F(I_{charging}) - V_{QL}(I_{out}, I_{charging}) \approx V_{CC} - V_F + R_{ds} \cdot I_{out} \tag{C.3}$$

From equation (C.3) the charging voltage depends on the voltage across the lower switch Q_L, and thus on the output current and on-state resistance. The current dependency of the charging voltage impacts the charging time required for the bootstrap

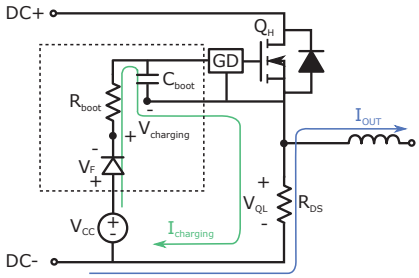

Figure C.2: Equivalent schematic presenting the charging state of the bootstrap with Q_L conducting.

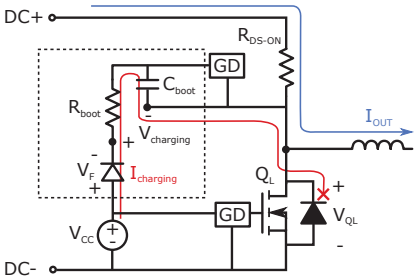

Figure C.3: Equivalent schematic with Q_H conducting.

circuit. The charging time of the bootstrap circuit can be calculated from equation (C.4). The output current is assumed to be constant during a switching period, which is a valid assumption for an inductive load.

$$t_{charging} = -ln\left(\frac{1-\frac{v_{boot}(t)}{V_{CC}-V_F+R_{ds}\cdot I_{out}}}{1-\frac{v_{boot}(0)}{V_{CC}-V_F+R_{ds}\cdot I_{out}}}\right)\cdot R_{boot}\cdot C_{boot} \tag{C.4}$$

As compared to equation (C.2), equation (C.4) depends on the voltage drop across switch Q_L, V_{CC} and required charging voltage of the bootstrap capacitor. The charging time presented in equation (C.4) is from $V_{boot}(0)$ to $V_{boot}(t)$. The limiting case of the bootstrap operation is where the bootstrap is charged from the minimum bootstrap voltage by the voltage drop occurring during a switching period. With the time required for charging the bootstrap obtained, the modulation index limit can be calculated as a function of the output current. The modulation index limit for a half bridge is given in equation (C.5).

$$M_a = \frac{T_s - t_{charging}(I_{out})}{T_s} \tag{C.5}$$

The current dependency of the modulation index limit and charging voltage described in equation (C.3) and equation (C.5) are shown for a half bridge in figure C.4. The active switching states do not dependent on the modulation index, the charging voltage are, as a consequence, only dependent on the output current, as is shown in figure C.4. The modulation index limit for a switching frequency of 50kHz is 0.8 using the conventional method in equation (C.2) compared to a peak value of 0.99 when considering output current and R_{ds} in equation (C.5). The method proposed does not take into consideration the reverse recovery of the bootstrap diode, temperature dependency of on-state resistance, parasitic inductance and blanking time [10]. Compared to the conventional method, the proposed mathematical approach takes into consideration the voltage drop introduced by the bootstrap diode and the bottom switch, when evaluating the bootstrap charging time. Taking into consideration the dependency of the charging voltage is essential for evaluating the applicability of a bootstrap circuit.

If a substantial voltage drop appears across the bottom switch, the bootstrap circuit could experience an over or undervoltage dependent on the current direction. As an example we can consider a reduced charging voltage, which appears when conducting a negative output current. During conduction of a negative output current the voltage drop across the bottom transistor and the forward voltage drop of the bootstrap diode are subtracted from the charging voltage as is described mathematically in equation (C.3) and visualised in figure C.4. Depending on the size of the voltage drop, the top switch will increase conduction and switching losses, potentially causing thermal runaway or triggering of the under voltage lockout. Both scenarios will impact reliability or prevent normal operation.

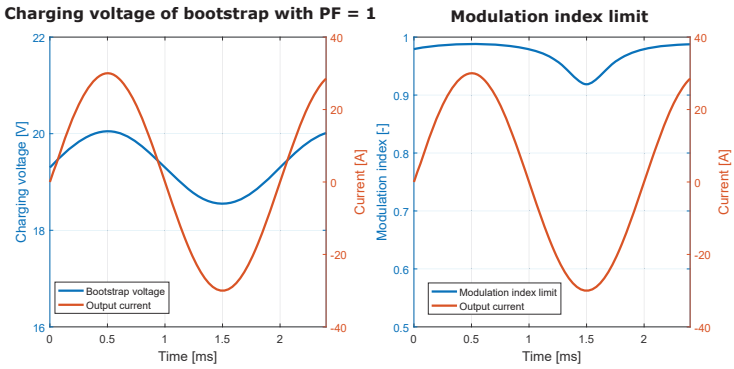

Figure C.4: An example of the bootstrap voltage and modulation index limit for a half bridge converter using the analytical approach.

The proposed mathematical approach is applicable for multilevel converters as well. With a more precise calculation method to evaluate the applicability of a bootstrap, a new investigation of a novel bootstrap circuit for a T-type converter will be performed. Multilevel converters as the T-type can significantly benefit from the use of a bootstrap circuit due to the increased number of isolated DC/DC converters needed.

Case study of a T-type converter

For multilevel topologies, the bootstrap is typically supplied by a DC/DC converter, referenced to the lower DC-rail [8], [11]. The charging states for such converters requires the bottom switch to be conducting. For multilevel topologies as the T-type, the bottom switch is only conducting during the negative half cycle of a fundamental output period. The disadvantages are large bootstrap capacitors, and a lower limit for the output frequency of the converter. A new bootstrap topology is proposed, introducing additional charging states compared to the typical bootstrap circuit. The bootstrap circuit proposed results in a reduction of 3 DC/DC converters compared to the conventional three phase solution without bootstrap. The bootstrap circuit can be seen in figure C.5. The bootstrap capacitor is charged by the isolated DC/DC converter

powering the middle leg.

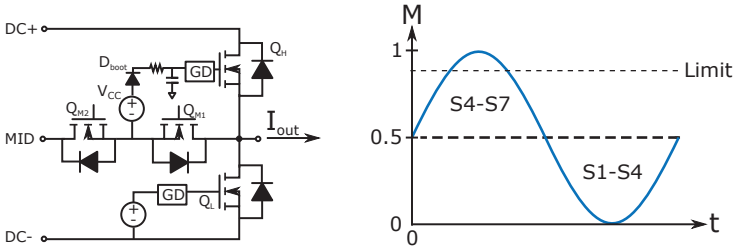

Figure C.5: Bootstrap circuit connected to floating supply from the middle leg.

By connecting the bootstrap to the middle leg, additional charging states are introduced when the middle leg (Q_{M1} and Q_{M2}) are conducting. The bootstrap circuit is comparable with the two level bootstrap circuit, when considering the middle and top leg interaction. The switching states are illustrated in figure C.5 with the respective charging states specified in table C.2. The voltage equation are obtained using the same method as for the two level converter. Switching state 2 is current independent, due to Q_{M1} not conducting the output current. The voltage drop across switch Q_{M1}, caused by the charging current, is neglected in the voltage equation.

Table C.2: Charging state for a bootstrap connected to the middle leg supply.

	Q_L	Q_{M1}	Q_{M2}	Q_H	**Effect on C_{boot}**	**Charging voltage**
S2	on	on	off	off	Charging	$V_{charging} = V_{cc} - V_F$
S3	off	on	off	off	Charging	$V_{charging} = V_{cc} - V_F$ if $I_{out} > 0$ $V_{charging} = V_{cc} - V_F + R_{ds-on} \cdot I_{out}$ if $I_{out} < 0$
S4	off	on	on	off	Charging	$V_{charging} = V_{cc} - V_F + R_{ds-on} \cdot I_{out}$
S5	off	off	on	off	$I_{out} > 0$ Charging $I_L < 0$ Discharging	$V_{charging} = V_{cc} - V_F + R_{ds-on} \cdot I_{out}$
S6	off	off	on	on	Discharging	
S7	off	off	off	on	Discharging	
S1	on	off	off	off	Discharging	

As can be seen from table C.2, the bootstrap is charged when the bottom and middle switches are conducting. Maintaining a charging state when conducting the lower switch (Q_L) prevents an under modulation limit. The equation for calculating the modulation index limit is different for a three level converter compared to a two level. The difference is the changing of switching states, depending on the modulation index. Taking the additional switching states into consideration, the equation for the modulation index limit for a T-type is given as equation (C.6).

$$M_a = \frac{T_s - t_{charging}(I_{out})}{2 \cdot T_s} + 0.5 \tag{C.6}$$

When a modulation index is below 0.5, the active switching states are 2 – 4. The upper switch (Q_H) is not actively switching, resulting in a reduced power consumption.

A lower limit is as a consequence present in the modulation index of 0.5, as seen in equation (C.6). The lower modulation index limit is also valid in the extreme case, of the C_{boot} voltage being zero, switch Q_L, Q_{M1} and Q_{M2} are still powered by the DC/DC converters. With a modulation index above 0.5, the active states are 4 to 6. The same relationship as is the case with the half bridge converter can be identified. The bootstrap is not charged during the conduction of the upper switch. The switching state introduces the $(T_s - t_{charging}(I_{out}))/(2 \cdot T_s)$ term. As an example the modulation index limit for a power factor of 0.7 is plotted in figure C.6 with the design parameters presented in table C.3.

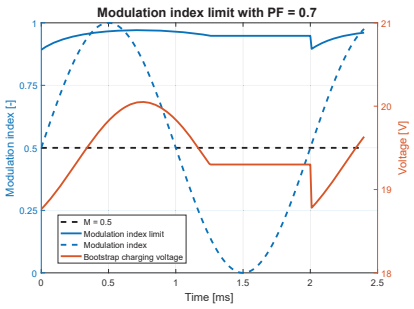

Figure C.6: Modulation index limit for an output peak current of 30 A, using the analytical approach.

Table C.3: Design parameters.

Parameter	Value
V_{min}	18V
C_{boot}	1μF
R_{boot}	5Ω
V_f	0.7 V
f_{sw}	50kHz
R_{ds-on}	25mΩ
f_{fund}	500 Hz
$I_{out-peak}$	30A
Q_g	161nC
$I_{supply+lkg}$	6mA

In figure C.6 the modulation index limit is shown with the comparison of a sinusoidal modulation waveform with an amplitude of 1. As was the case with the half bridge, during postive current amplitudes, the bootstrap voltage is increased. The increase in the bootstrap voltage can be identified by the increase of the modulation index limit between 0.2 and 1.2ms. With a modulation index below 0.5 and a negative current, the modulation index limit is constant. The modulation index is constant due to the fact that all active switching states are charging the bootstrap capacitor and the power consumption of the circuit is reduced. With the modulation index above 0.5 with a negative current, the voltage across Q_{M1} is reducing the charging voltage of the bootstrap. The effect of operating above the modulation index limit depends on the power consumption of the circuit and the size of the bootstrap capacitor. The bootstrap will be discharged during the time of the modulation index surpassing the limit.

Numerical verification of bootstrap design rules

To ensure the mathematical analysis is applicable, an electrical simulation is designed with the parameters given in table C.3. The modulation index limit is analytically calculated in figure C.6 to be 0.97 with an output current of 30A, ensuring a minimum bootstrap voltage of 18V. To validate the math, an electrical model simulating the steady state bootstrap voltage is used. In the simulation an open loop control is used

to operate ideal switches with an on-resistance of 25mΩ. The bootstrap circuit is connected to an electrical model of the gate driver circuit. The model of the gate driver includes quiescent and leakage current and a switching network charging/discharging an input capacitance of a MOSFET. The charging and discharging of the MOSFET input capacitance is determined based on the control signal to the top switch (Q_H). The modulation index is swept from 0.5 to 1 and the minimum bootstrap voltage is extracted. The bootstrap voltage as a function of the modulation index is shown in figure C.7 at different current values.

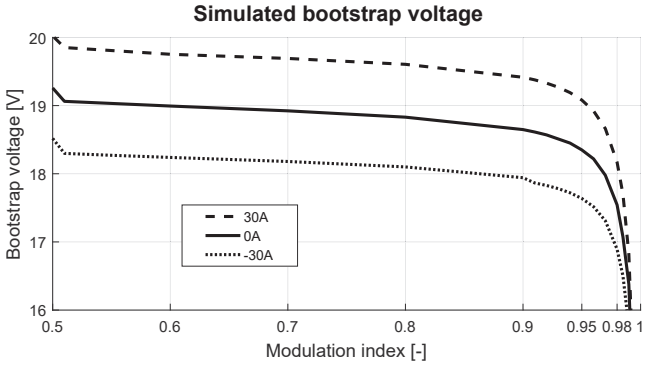

Figure C.7: Minimum voltage of the bootstrap circuit under different modulation indexes and output currents.

From figure C.7, it can be identified that from the numerical circuit simulator a modulation index of 0.98 with 30A of output current results in a minimum bootstrap voltage of 18 V. Increasing the modulation index above 0.98 results in a steeply decreasing bootstrap voltage. For a modulation index of 0.99 the voltage is decreased below 17 V.

A comparison between the different methods of calculating the minimum charging time are converted into modulation index limits in Table C.4. The results are obtained using the design parameters specified in table C.3 as a reference point.

Table C.4: Modulation index limits calculated with different methods for a T-type converter.

Current = 30A	**$t_{charge} = 5 \cdot \tau$ [7],[12]**	**$t_{charge} = 4 \cdot \tau$ [5],[6]**	**$t_{charge} = 2.3 \cdot \tau$ [8]**	**Proposed Method**	**Simulated**
Modulation limit	0.5	0.5	0.71	0.97	0.98
Error	0.48	0.48	0.27	0.01	0

As can be seen from table C.4, an accurate prediction of the modulation index limit is obtainable using the method described in this paper. Based on the simulated result in figure C.7 and table C.4, the mathematical analysis is validated. The estimated charging time for the conventional methods are a substantial underestimation of the modulation index limit. The comparison confirm the validity of the proposed method

for evaluating the applicability of the bootstrap circuit. For the conventional methods a bootstrap circuit for a T-type converter would have been deemed inappropriate due the low modulation index limit, however the new mathematical approach and numerical simulation present safe operation with a very high modulation index for the proposed bootstrap circuit. Underestimating the bootstrap modulation index, introduces a safety margin, which is not present in the proposed method. In practice the modulation index limit, should be selected lower than the estimated limit. Introducing a safety margin accounting for temperature dependencies and parameter variations during the useful life.

Conclusion

A general mathematical approach for calculating the modulation index limit is derived. The analytical model takes diode forward voltage, transistor on-state resistance, switching frequency, power factor and current into consideration. The mathematical approach is used on a proposed bootstrap circuit of a three level, T-type converter. The proposed bootstrap circuit is independent of the fundamental output frequency, making it comparable to the well establish bootstrap circuit for a half bridge. The model is validated using a circuit simulator, which simulates the bootstrap voltage under steady state conditions. The simulation results are in good agreement with the analytical result, compared to other calculation methods. A novel T-type bootstrap circuit is designed with a high modulation index limit, ensuring safe operating conditions in regards to the bootstrap voltage. The proposed bootstrap circuit is capable of reducing the number of isolated DC/DC converters from seven to four, while maintaining the advantages of having a switching frequency dependent charging cycle. The T-type bootstrap circuit is also increasing the modulation index limit, compared to a half bridge module with similar switching frequency and bootstrap design parameters. The approach presented allows the designer to accurately estimate the modulation index limit and assessing the applicability of a bootstrap circuit in a given application.

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Appendix D

Digital design of a converter using 3D models and finite element software

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Digital design of a converter using 3D models and finite element software

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Keywords

Semiconductor device packaging, power semiconductor devices, power converter, circuit simulation.

Abstract

Power electronics are used in a wide range of applications, where efficiency and power density are crucial parameters for optimization. New wide-bandgap devices are used with multilevel topologies to push efficiencies and power densities. The fast switching devices requires a compact layout, to utilize their potential. Validating layout performance experimentally is a challenging task. The measurement nodes are often inaccessible due to the compact layout. An accurate digital representation is therefore useful in a design phase to access performance and for performing design iterations. In this paper, a digital representation of a T-type converter is created using FEM extraction of 3D geometry and material structures of the converter. The model includes semiconductor models, parasitics from PCBs, passive components and power module. The parasitics from PCBs and power module are extracted using ANSYS Q3D Extractor. After digital design iterations, a converter is built. The performance is measured and compared to the model, using accessible measurement nodes. Very good agreement between simulated and measured waveforms are obtained. Deviations in dV/dt during turn on is observed. Deviations between SiC models and experimental IV-curves are identified, as the cause of deviation. The implications of switch detail mismatch on the digital representation is discussed.

Introduction

Power electronic converters are used in a wide range of applications from energy generation and transportation to electrical household appliances. The power handling capability of these converters varies from mW to the MW range. With increasing power handling capability, the efficiency and power density become crucial subjects for optimization. An efficiency increase is desired in relation to reliability, operation

economy and to reduce cooling requirements [1]-[3]. The power density is a desired optimization object with respect to reducing the size of the converter solution. A size reduction implies a reduction of raw materials of the converter, which saves valuable space and weight, making installation and transportation of the converter more convenient. Applications where smaller size and light weight are priorities, include portable electronics, data center cabinets, airplane, wind turbine and electrical drive applications [4],[5]. One parameter effecting efficiency and power density, is the switching frequency. Higher switching frequencies increases the power dissipation of the semiconductors, resulting in a larger cooling requirements [6]. When considering the passive components, it is ideal to have as high a switching frequency, as possible, to reduce the size of passive components. The switching frequency of a converter is as a consequence selected based on efficiency and a compromise between the heatsink and passive components volume [7]. The Si technology used in todays converters, often introduce large switching losses, when considering hard switched topologies. The large switching losses results in the size of a converter system typically being dominated by the passive components and the heatsink. The new wide band gap materials, such as Silicon Carbide (SiC) are therefore specifically promising, since they achieve significant lower switching losses and R_{ds-on} values for the same blocking voltage [8]. The lower switching losses allows the converters to operate with a higher switching frequency, reducing the size of passive components while maintaining a high efficiency [9]. The new WBG devices are as a consequence expected to introduce a paradigm shift by significantly improving the power density and efficiency of existing converter products [10],[11]. The low switching losses are obtained by having fast switching transients, with transitioning times in the range of tens of nanoseconds [12]. The disadvantage of the fast switching transients are the large rate of changes introduced (dI/dt and dV/dt). The larger dI/dt and dV/dt introduces challenges for the converter control, design and measurements [13]-[18]. During the design phase, it is important to perform design iterations based on the layout performance during high dV/dt and dI/dt events, to ensure mitigation of over voltage and false turn on [8]. Failing to accurately simulate critical operation scenarios will result in design iterations including a physical prototype. Having a physical prototype as part of a design iteration is expensive and time consuming. An additional advantage of an accurate digital design process is related to the challenge of extracting information from a physical prototype without affecting the performance and switching transients. A few nH or pF of parasitic impedance may substantially effect the measured waveform [19]-[21]. Furthermore many of the measurement points of interest are inaccessible due to the physical layout. The challenges with measuring waveforms, complicates the validation of the converter performance. An accurate digital representation of a design therefore becomes an essential tool, in evaluating layout performance, obtain physical inaccessible information and performing digital design iterations, saving cost.

In this paper a digital representation and validation of a converter is presented. The digital representation relies on parasitics extractions of power/gatedriver PCBs as well as power modules using 3D finite element software combined with SiC MOSFET models and measured parasitics of passive components. The combination of all these elements allows a number of key design choices to be optimized such as choosing the

right passives that will match the parasitic elements. For the present study the digital design process is used for the case of optimizing inductance and passives selection for a T-type converter used for drive application. The T-Type converter was identified in a previous work as an optimum topology for a 7.5kW inverter in drive applications [11]. The selection of a T-Type converter is based on the high efficiency and power density obtained, with the addition of only two semiconductors per phase. The schematic of a T-type converter is shown in Figure D.1. The T-type introduces an additional output voltage level and reduced switching voltage, compared to the commonly used half bridge topology. The reduced voltage is an advantage compared to switching losses and false turn on mitigation. The T-type requires a total number of four switches per phase. Two switches rated for the full DC-link voltage for the top and bottom switch. The middle leg requires two switches rated for half the DC-link voltage. The power loop of a T-type encloses three MOSFETs, a top or bottom switch and two middle switches. The power loop inductance is as a consequence larger than for a half bridge, making the topology prone to switch over voltages [22].

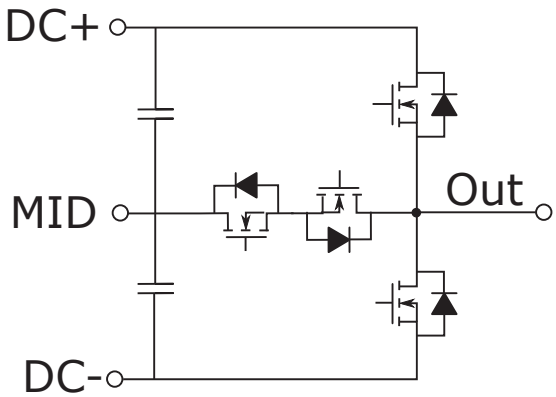

Figure D.1: Circuit schematic of a T-type converter.

The digital design iterations are therefore performed to minimize the power loop inductance, reducing the switch over voltage. Research on optimizing the power module layout to reduce power loop inductance or output capacitance for a half bridge to a minimum, has prevopisly been studied [23]-[25] using a 3 dimensional module layout. Previous publications are focusing on simulating the power module parasitic, while this paper also includes the signal routing PCBs. The signal routing PCBs are crucial to address, since they might contribute with dominant parasitics, severely affecting the switching performance. The focus of this paper will be on the parasitic extraction of a full T-type converter layout, and how the information is used to perform digital design iteration. With the increase level of detail for the digital representation, this paper quantify the values of parasitics introduced from power routing PCBs, gate drivers and power module. Quantifying the parasitic shows the PCB routing parasitics have significant impact on switching performance and EMI generated. The accuracy of the digital representation is experimentally validated by performing static and dynamic

measurement of the T-type power module and bare MOSFET dies. Based on the experimental measurements the accuracy of the digital twin is evaluated and discussed.

Digital representation and assumptions

The digital representation is based on the parasitic network extracted from the geometric layout and material information, measured impedance of passive components and a MOSFET model supplied by the manufacture [26]. A flowchart of the software used in developing the digital simulation is shown in figure D.2, together with the design iteration feedback.

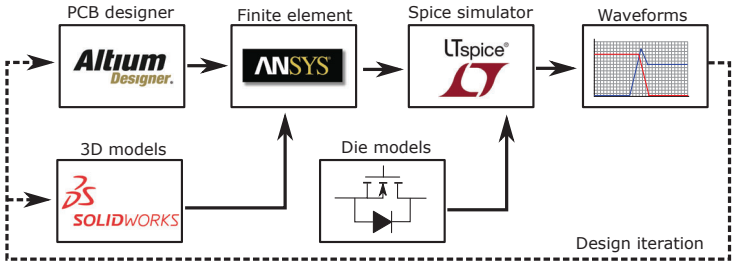

Figure D.2: Flowchart of the simulation tools and models used for the digital design process

In the following section the assumptions made in the modelling and the justification of them will be presented.

MOSFET modelling

The schematic of the MOSFET model utilized is presented in Figure D.3. The model is based on a generic power MOSFET model taking into consideration the device capacitances, the voltage dependency of the output capacitances, the temperature dependence of the drift resistance and the threshold voltage [27].

The current source I_D is dependent on the gate-source, drain-source and the temperature dependent threshold voltage [28]. The function describing the drain current used in the model is a compromise between simplicity and precision, enabling fast computation in simulations [29]. The parameters of the functions are selected to fit the typical IV-characteristics of the MOSFET. Likewise is the voltage dependency of the output capacitance fitted to the typical capacitance characteristics of the MOSFET. The body diode modelling is included in the MOSFET model from the manufacturer. The diode model used is the standard Berkeley SPICE semiconductor diode model, which does not include the gate-voltage dependency of the body diode forward voltage. The body diode is utilized for free wheeling during deadtime, neglecting its gate voltage dependency will only result in a minor reduction of estimated semiconductor losses. A model representing the characteristics of a typical MOSFET is selected, due to the inherent complexity increase in having a MOSFET model for each device.

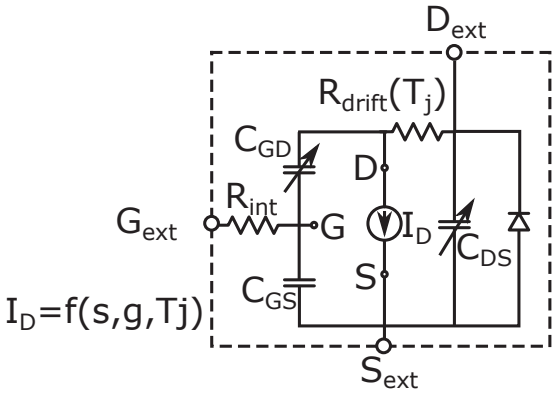

Figure D.3: Circuit model of a power MOSFET.

Gate-driver IC modelling

In the simulation the rise and fall time of the Gate driver IC is neglected, due to the low pass filter effect of the gate loop. The IC transient can be neglected due to gate loop bandwidth being lower than the frequency content of the IC rise and fall times [30]. The electrical diagram of the gate loop is shown in Figure D.4, including parasitic impedances.

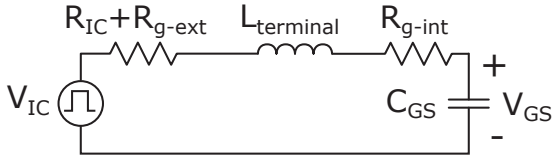

Figure D.4: Circuit model of the gate-loop with neglected gate-drain capacitance and PCB inductance.

The bode diagram of the gate-loop is shown in Fig. D.5 with the bandwidth of the measured IC rise time specified.

In the bode diagram, the gate-source capacitance, inductance from power module terminals, internal, external and IC resistances are taken into consideration. The IC resistance is included, since a low external gate resistance is used, and the resistance value is comparable to the internal gate resistance. The inductance contribution from PCB and DBC layout is omitted due to the dominant contribution being from the terminals, as will be presented in section Design iterations on power module. Including the neglected inductances will decrease the cut off frequency, providing a higher attenuation of the IC transients. Since the frequency content of the rise time has a gain of -5dB, it can be neglected from the simulation model, without effecting the switching behaviour of the MOSFET.

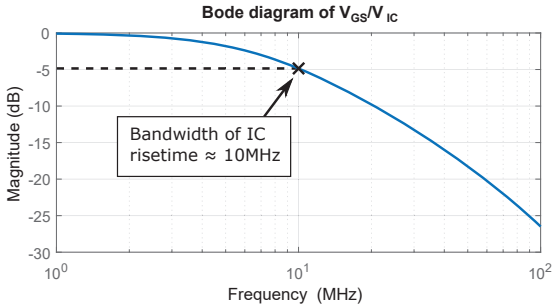

Figure D.5: Magnitude response of the gate loop. V_{GS}/V_{IN}.

Design iterations on power module

The scope of this paper is performing digital design iterations using a digital model, and to experimentally validate the digital model using a physical prototype. The scope of the paper are as a consequence not limited by the packaging technology selected. For the initial prototype the packaging technology, housing and terminals were locked for pragmatic reasons. The packaging technology selected, utilizes bondwires as research has proven that conventional packaging technology can achieve clean switching waveforms, by carefully considering the layout [31]. The minimization of the gate-source loop inductance is not prioritized, due to the dominant inductance being contributed by the power module terminals. Initially a gate resistance of 7Ω and 2 Ω are selected for the turn on and turn off gate resistance, respectively. The selection of gate resistance ensures immunity in regards to miller induced false turn on [32]. The power module is intended to operate with a switching frequency of 70 kHz. Having external free wheeling diodes are therefore not considered as an option for the T-type power module. The reduction in conduction losses during free wheeling from the external diodes, are not justified by the increase in switching losses associated with the additional output capacitance introduced. When designing a power module, the first step is creating an initial design, upon which digital design iterations are performed, until a satisfactory layout is achieved. In this paper an example of a design iteration in the final design stage of the power module is presented. The design iteration is performed with focus on minimizing the power loop inductance for both loops, to minimize the switch over voltages, a T-type converter is prone to experience. The power module layout is shown in Figure D.6 with the parasitic self inductances extracted in Figure D.7 using Ansys Q3D. The self inductance is extracted at a frequency of 100 MHz.

If the self inductance of the power loops are summed together, the inductances becomes 3.9nH and 4.7nH for power loop 1 and 2 respectively. Power loop 2 will as a consequence be the limiting loop when considering switch over voltage. The cause of the higher inductance is a combination of the thin trace width between the upper MOSFET and the ceramic capacitor and the long DBC trace between the MOSFETs in the middle and upper leg. Based on the knowledge gained from the self inductances, a design iteration is performed to minimize the inductance of power loop 2,

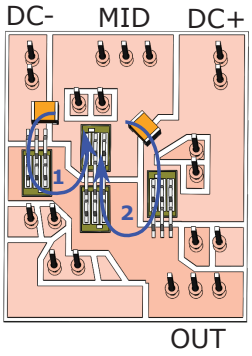

Figure D.6: Power module design with capacitive snubber.

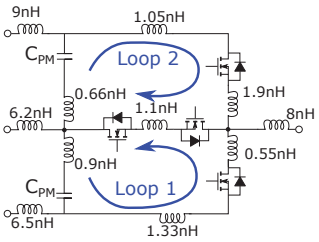

Figure D.7: Self inductance extracted from power module with C snubber.

without increasing the inductance of power loop 1 significantly. The adjustments are a decrease of the loop length and increase of trace width together with the inclusion of damping resistors in the DC-link snubber. To enable the soldering of a damping resistor, a small copper island is needed, which were not present in the initial layout. The layout after a design iteration can be seen in Figure D.8 with the self inductance presented in Figure D.9. Power loop 1 maintains roughly the same path, while power

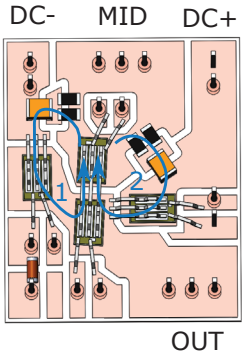

Figure D.8: Power module design with RC snubber and reduced power loop inductance.

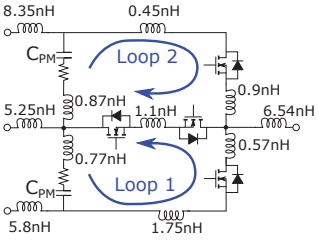

Figure D.9: Self inductance extracted from power module with RC snubber.

loop 2 is significantly reduced in length. The effect can be seen by summing up the inductances in Figure D.9. The inductances for power loop 1 and 2 are 4.3nH and 3.3nH respectively. The inductance is reduced in power loop 2, even with the additional inductance contributed by implementing a damping resistor. In figure D.10 a side-by-side comparison is presented for the power module layouts and their DC-link

snubber configurations.

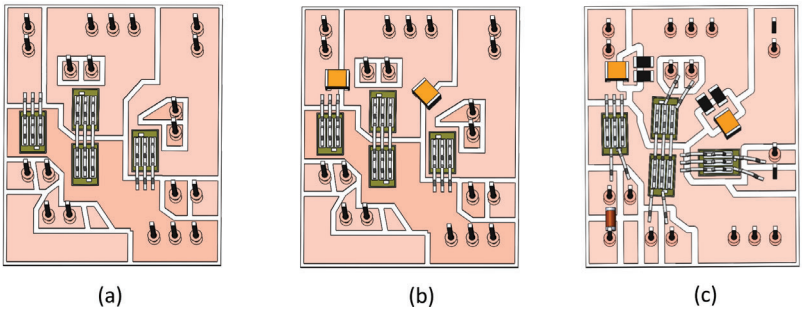

Figure D.10: Side-by-side comparison of power module layout iterations.

To evaluate the performance of power module layout (a),(b) and (c), an electrical simulation is performed. The switch overvoltage is simulated in LTSpice including parasitic inductances, couplings and capacitances from the module as well as the power and gate driver PCB – based on Q3D simulations of each of these structures. The extracted information is combined with the die model as well as the properties of the used passive components, the latter of which was obtained from LCR measurements. In Figure D.11 the voltage overshoot of the lower switch is presented for each design. The simulation is performed with a DC-link voltage of 800 V, which is the maximum expected DC-link voltage under normal operation.

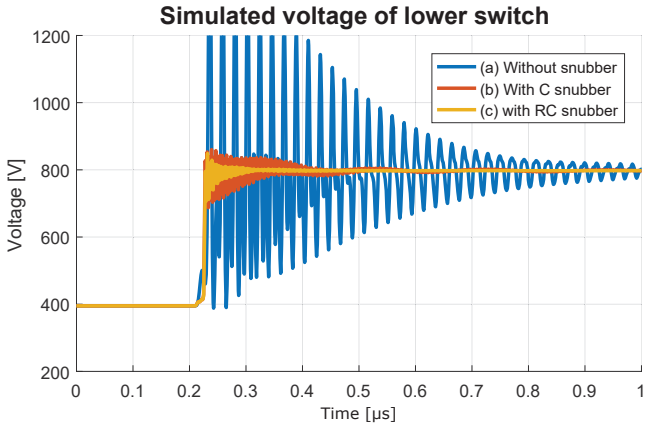

Figure D.11: Simulated voltage overshoot of the lower switch.

From Figure D.11 a voltage overshoot above 1.2kV can be observed for the power module without a capacitive snubber circuit. The electrical simulation provides proof for the need of a capacitive snubber inside the power module. Two different capacitive snubber circuits are investigated with and without a damping resistor. The voltage overshoot is reduced to 860V and 848V for a C and RC snubber respectively. The

simulated voltage overshoots with a DC-link snubber are below the 1.2 kV voltage rating of the SiC MOSFET. Both snubber circuits produces an insignificant voltage overshoot compared to the DC-link voltage of 800 V. The impact of the damping resistor can be identified by the increased damping factor of the high frequency ringing, resulting in reduced switching noise. Design (c) with the RC-snubber reduces voltage overshoot and conducted EMI, making it the best performing layout out of the three. Additional design iterations to minimize inductance will introduce insignificant improvements in regards to switch over voltage. The semiconductor devices are placed in near proximity to each other to obtain a low power loop inductance. Having semiconductors in near proximity increases their thermal coupling, reducing the thermal performance. The distance between semiconductor dies are a compromise between switching and thermal performance. To improve the thermal performance of the power module, Aluminum Nitride (AlN) is used as DBC ceramic, which has a high thermal conductivity. The combination of high thermal conductivity, reduced switching losses and distributed power dissipation of the T-type topology ensures safe operation temperatures during normal operation. Selected parasitic capacitances and inductances extracted from the design iteration with an RC snubber are summarized in Table D.1, including parasitics from power and gate driver PCB. An electrical schematic of the parasitic capacitances and self inductances from Table D.1 is shown in Figure D.12.

Table D.1: Extracted parasitics of power module and PCB boards at 100 MHz.

Impedance	**Value**	**Path**
L_{DC+}	8.35nH	DBC + Terminal
L_{MID}	5.25nH	DBC + Terminal
L_{DC-}	5.8nH	DBC + Terminal
L_{OUT}	6.54nH	DBC + Terminal
L_{D4}	0.45nH	DBC
L_{D1}	0.57nH	DBC
L_{S4}	0.9nH	DBC
$L_{S,2-3}$	1.1nH	Bondwire
L_{S1}	1.75nH	DBC + Bondwire
$L_{MID,DC+}$	0.87nH	DBC + Component
$L_{DC-,MID}$	0.77nH	DBC + Component
$C_{OUT,Base}$	45pF	DBC
$C_{DC+,Base}$	29pF	DBC
$C_{MID,Base}$	36pF	DBC
$C_{DC-,Base}$	11pF	DBC
L_{G-S}	14.9 nH	DBC + Terminals
$L_{Gate\,driver}$	2.9 nH	PCB
$L_{PCB:DC+,MID}$	14.5 nH	PCB
$L_{PCB:MID,DC-}$	14.7 nH	PCB

The internal DC-link snubber is placed inside the power module, due to the significant inductance contributed by the terminals (L_{DC+},L_{MID} and L_{DC-}). The internal

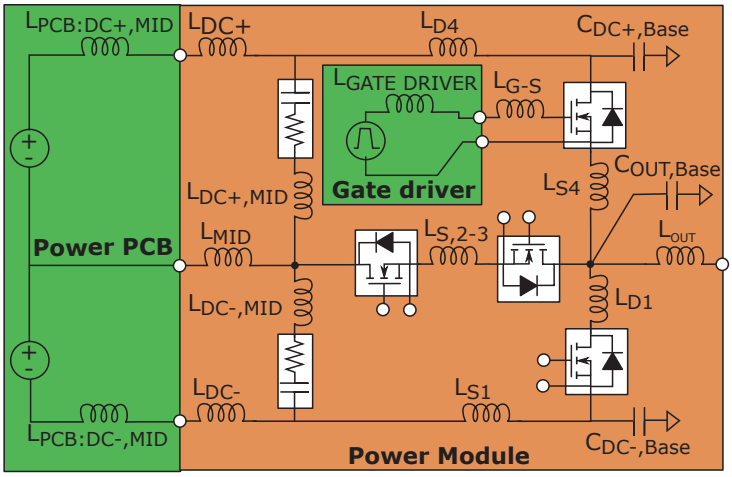

Figure D.12: Electrical schematic with self inductances and capacitance contributions from the converter layout. The mutual couplings of the parasitics are omitted for simplicity.

DC-link snubber provides a low impedance path, for the high frequency switching currents. The capacitors thereby enables switching with a higher dI/dt without generating hazardous switch over voltages, as was shown in Figure D.11. The inductance introduced by the distance between dies and DC-link terminals are then less critical for switch overvoltages, due to implementation of a DC-link snubber. Dedicated design iterations with the objective of minimizing the inductance between terminals and dies are therefore not performed, as the dominant inductance is contributed by the terminals and only a minor impact on the switching performance will be achieved. A disadvantages with having a distributed DC-link is the potential of creating resonance circuits with a low damping factor between internal and external capacitors. If the resonance is not damped it will be reflected at the output voltage, potentially causing switch over voltages or increased EMI. If a too large damping resistor is selected, it will likewise cause switch over voltages.

Selecting DC-link damping resistor

The decoupling capacitors placed inside the power module creates a resonance circuit with the terminal inductance and the external DC-link capacitors (C_{DC}) or DC voltage source. The internal decoupling capacitors have a low capacitance value of 50nF at the full DC-link voltage. The capacitance value is small since the purpose of the internal DC-link is not to store energy, but to create a low impedance path for the high frequency power loop currents. The resonance circuit between the external and internal DC-link is excited by the switching of the MOSFETs. It is desired to dampen the resonance to reduce the amplitude and duration of the ringing. The optimum resistance can be selected using equation (D.1) for the decoupling capacitor connected

betweeen MID and DC+. The optimum resistance is determined based on having a minimum voltage overshoot and a high damping factor [14].

$$R_{opt} = \frac{1}{2} \cdot \sqrt{\frac{L_{DC+} + L_{MID} + L_{MID,DC+} + L_{PCB-DC+,MID}}{C_{pm}}} \tag{D.1}$$

The power module capacitance is selected during the design phase, where as the stray inductance is extracted from the power module and PCB layout. With the parasitic inductances and AC resistance values extracted, a damping resistor of 280mΩ is calculated as the optimum. The inductance contribution from the power routing PCB is substitutional and neglecting it, when selecting a damping resistor will result in increased EMI and switch overvoltages. The response with and without damping resistor can be seen in Fig. D.13.

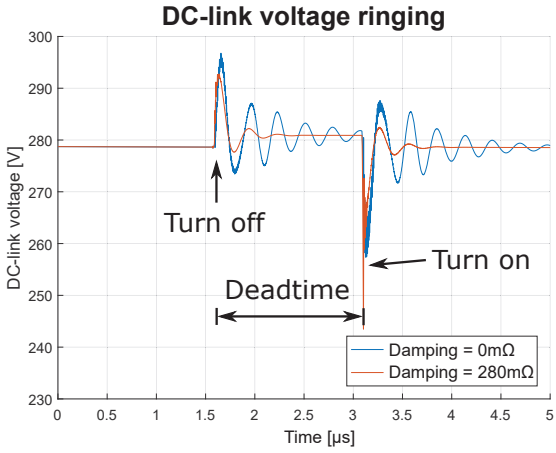

Figure D.13: Simulated DC-link resonance with and without damping.

As is visible from Figure D.13 the voltage overshoot is reduced from 296 V to 286 V during turn on, with a DC-link voltage of ±280 V. The damping resistor also effectively dampens the resonance after two ringing periods. The parasitic extraction has proven itself useful in selecting a damping resistor based on the physical realization of the converter.

Physical prototype

A single prototype is build based on the final design shown in Section D to perform an experimental validation of the digital model. The prototype of the power module can be seen in Figure D.14 without gel and housing.

It may be noted that a small modification of the bondwire location for the top MOSFET was needed, due to manufacturing tolerances of the equipment. Only a small inductance contribution from the twisting of the bondwire is expected, with

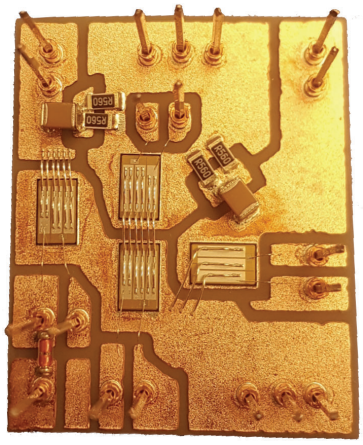

Figure D.14: Picture of the physical power module based on design iteration two.

minor impact on switch over voltages. An experimental setup is therefore build using the power module.

Experimental results

The experimental results is obtained by performing a double pulse test. A T-type converter can be configured to perform a double pulse test by keeping one of the middle leg switches on, while providing PWM pulses to the top switch as shown in Figure D.15. The measurements are performed using a 500 MHz passive voltage probe (Teledyne Lecroy PP026), a 50 MHz current probe (Teledyne Lecroy CP030) and a 1 GHz, high definition oscilloscope (Teledyne Lecroy HDO6104).

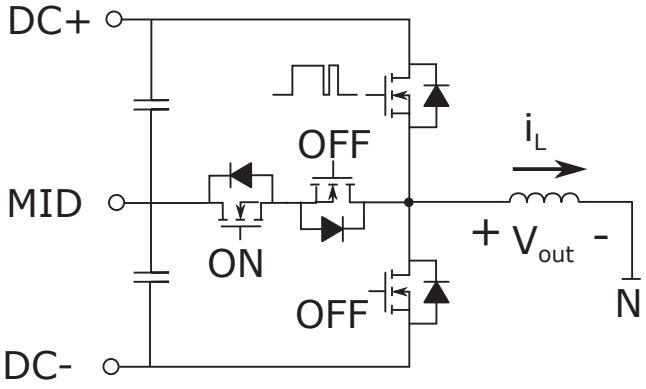

Figure D.15: Double pulse configuration without parasitic impedances included.

The measured output voltage and inductor current during a double pulse is shown

in Figure D.16.

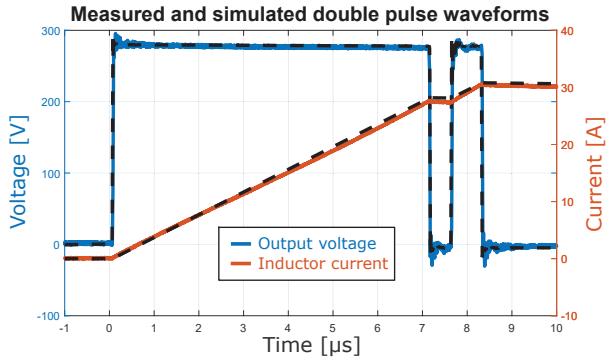

Figure D.16: Measured double pulse with a DC-link voltage of 560V, ramping current up to 30A. The dashed black lines are simulated waveforms.

The first turn on has a duration of $7\mu s$, ramping up the inductor current from 0A to 30A. At $7\mu s$ the top switch is turned off, and the inductor current free wheels through a body diode in the middle leg. After a short time duration in the free wheeling state, the top switch is turned on for a duration of $1\mu s$. Seen from Figure D.16 a small voltage overshoot occurs after the switching event, caused by the DC-link resonance. During the double pulse with 30A, the voltage overshoot reaches 287 V and is dampend within two ringing periods, coherent with the behaviour simulated. The measured resonance is in agreement with the simulation in regards to ringing frequency, amplitude and damping. Looking on a μs scale, a good agreement between measured and simulated performance is observed. The nanosecond behaviour of the model is analyzed using the measured and simulated output voltage during the switching transient as shown in Figure D.17 during turn on and off, with an inductor current of 30A.

Comparing the output voltages, a very good agreement is present during turn off of the top switch. The output voltage waveform during turn off is mainly controlled by the output capacitances of the SiC MOSFETs, the capacitance contributed by the layout and the output current of the inductor. When the top MOSFET turns off, the inductor gradually discharges the parasitic capacitors connected to the output. Comparing the waveforms indicates a good correlation between the simulated and physical capacitances values, where the dominant capacitance contribution is associated with the MOSFETs output capacitances. During the turn on switching a good agreement is present during the steady state conduction, but some deviation is observed during the rise time of the voltage. A dV/dt of 52 kV/μs is simulated, where 14 kV/μs is measured. Although the predominantly good agreement between digital representation and experiment demonstrates the applicability of the digital design process in reducing physical prototype iterations the dV/dt deviations are worth looking into since these can be crucial for accurately determining switching losses and switch over voltages before building a prototype.

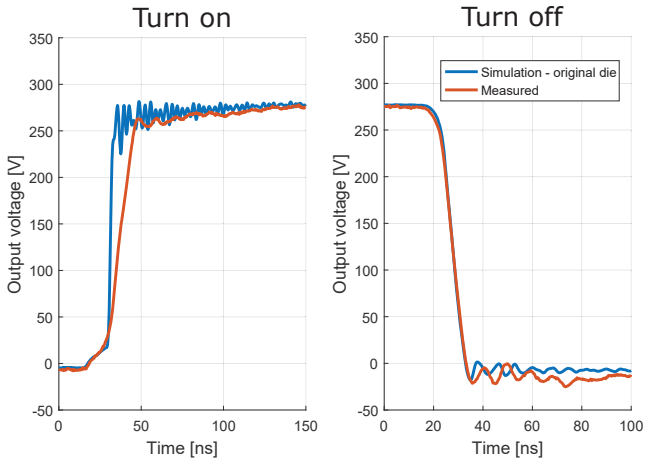

Figure D.17: Zoom of measured and simulated double pulse with an inductor current of 30 A.

Root cause analysis of discrepancies between digital twin and experimental measurements

To explain the discrepancies between measurement and simulation, two different hypothesis are investigated, which are addressed alphabetically in the following subsections. The first hypothesis being addressed is whether small geometrical differences between model and manufactured prototypes can affect the switching trajectory while the second hypothesis is whether inaccuracies in the applied die model can be the cause of the observed dV/dt discrepancies.

Deviations between geometric model and manufactured prototypes give significant parasitic deviations.

During assembly of the power module, the power loop bondwires were twisted for the top MOSFET. The bondwires were twisted to ensure a reliable bond to the DBC. A zoom of the twisted bondwire is shown in Figure D.18.

To quantify the impact of assuming the inductance contribution from twisted bond wires to be neglectable, the parasitics are extractor in ANSYS Q3D Extractor. The parasitics extracted showed that the twisted bonwdwires increases the self inductance from 0.9nH to 1.3nH. A 0.4nH difference in the power loop inductance increases the combined inductance by 13%. The impact of the small inductance increase is quantified by evaluating the voltage overshoot using the digital model. Based on the simulation results, the small inductance increase is not reflected on the output voltage or current, and is therefore not capable of explaining the discrepancy.

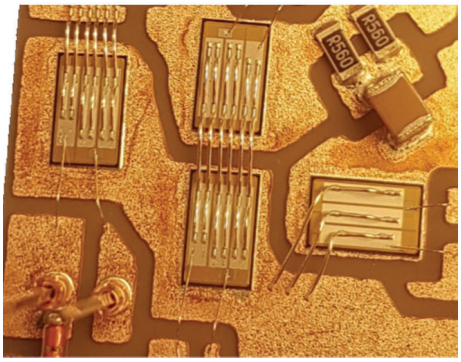

Figure D.18: Deviation in bondwire placement due to manufacturing tolerances.

Die characteristics are not modelled accurately

The initial assumption regarding the MOSFET model is that the model supplied by the manufacturer is a good representation of the physical device, and only small deviations are present in the physical MOSFET in respect to the MOSFET model.

IV-characteristics

This hypothesis is firstly challenged by measuring the IV-characteristics of the power module. The IV characteristics shown in Figure D.19 is the comparison between the IV-characteristics of the top switch and the simulation model.

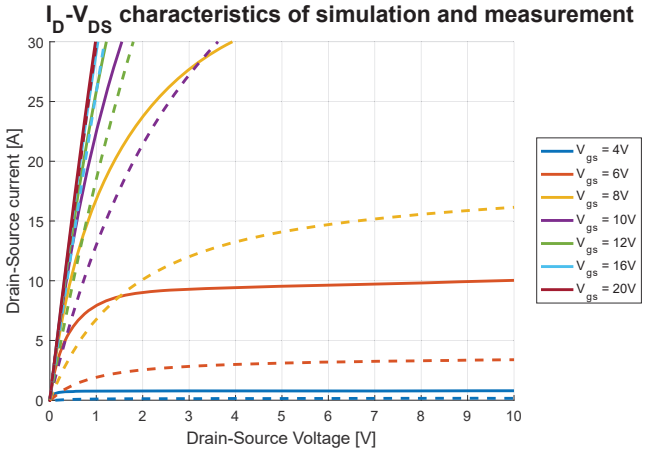

Figure D.19: The solid lines are IV-characteristics extracted from the MOSFET model and dashed are measured.

As can be seen a significant difference is present in the IV-characteristics between the simulated (Solid line) and measured (dashed line) MOSFET. Comparing the curves

in Figure D.19, a good agreement between the IV curves at gate voltages above 16V can be identified. A good match between measured and simulated drift resistance is therefore confirmed. The good agreement of the drift resistance, is in alignment with the accuracy of the simulation model in the μs range. However a significant deviation in both threshold voltage and shape can be identified for the curves below a gate voltage of 16V. A threshold voltage shift of approximately 2V can be identified. The physical device will as a consequence reach a higher gate-source voltage, before the channel conducts the full current. The gate current will as a consequence reduce, due to the reduced voltage differential. A lower gate current will result in a slower charging of the gate-drain capacitance and thereby reduce the switching dV/dt.

A deviation of 2V in the miller plateau, significantly impacts the voltage differential, but it cannot solely explain the factor 4 difference in dV/dt. With substantial deviations observed with a V_{DS} voltage below 10V, the IV-characteristics at larger drain-source voltages contains a high degree of uncertainty. The difference of the switching trajectory between the modelled MOSFET die and the physical device, could explain the factor of for in difference. Several MOSFET dies were measured using the fixture in Figure D.20, showing noticeable deviations in IV-characteristics from MOSFET to MOSFET.

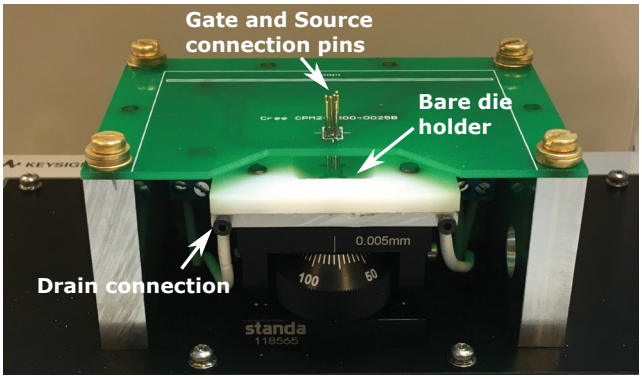

Figure D.20: Photograph of MOSFET die fixture.

Effect on switching trajectory

Based on the IV characteristic deviation, a parameter fit for the MOSFET is performed. The current equation depends on the gate-source and drain-source voltages, resulting in a surface fit. The IV-characteristics of the MOSFET during a switching transient is illustrated in Figure D.21, using the fitted IV-characteristics.

As indicated by the gray box in Figure D.21, the fit is performed upto a drain-source voltage of 10V. A high degree of uncertainty regarding the IV-behaviour at higher voltage is therefore present practically. Performing IV-characterisation upto higher drain-source voltages introduces a challenge, regarding power dissipation during measurement. As seen from Figure D.21, the miller plateau changes during the

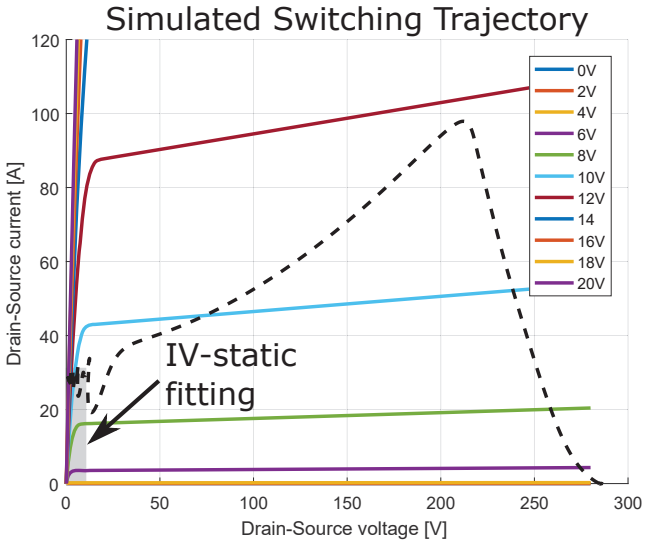

Figure D.21: Simulated switching trajectory in Ids-Vds characteristics.

switching transient. The result of the decreasing miller plateau, is the discharging of C_{GS}, increasing the current to the gate-drain capacitance (C_{GD}). In the simulation the current from C_{GS} is around 4.5A, which is approximately 4 times the current flowing through the external gate resistor. A deviation in IV-characteristics at higher voltages can as a consequence explain the increase dV/dt simulated. The general equation (D.2) is as a consequence not valid in the simulation model.

$$I_{gate} = C_{GD}(V_{GD}) \cdot \frac{dV_{GD}}{dt} \tag{D.2}$$

Having a model accurately predicting the MOSFET characteristics at higher voltages, therefore becomes crucial to accurately simulate the switching behaviour. Substantial parameter variations between MOSFETs, could provide an accuracy limit in determining switching losses, if individual MOSFET models are not used.

Capacitance measurement

The comparison between measured and simulated capacitance of the MOSFET model is tested, by measuring the capacitance of a MOSFET die, using the fixture in Figure D.20. The capacitance is not measured on the power module, due to the internal DC-link capacitor affecting the measurement. The measured and simulated output capacitance are shown in Figure D.22. The solid line is measured capacitance and the dashed line is simulated.

Seen from Figure D.22, a good agreement between experimental and simulated capacitances are observed. A good agreement is also expected, as the turn off transients between simulation and measurements are in good agreement. The capacitance

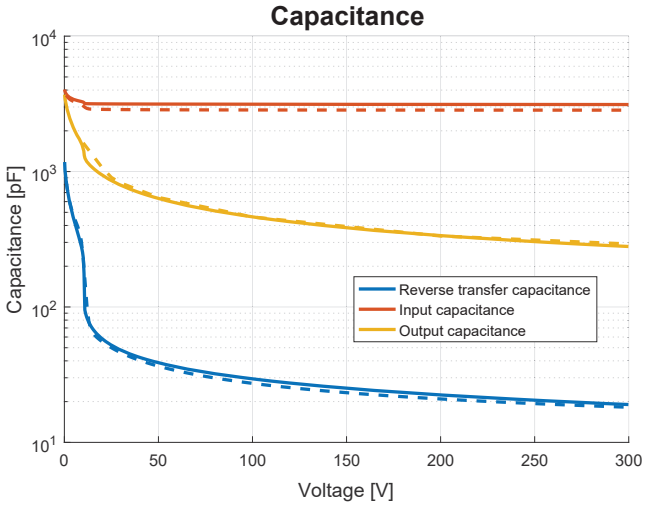

Figure D.22: Comparison between measured and modelled MOSFET output capacitance. Solid lines are measured and dashed are extracted from the MOSFET model.

of the MOSFET model is not the cause of deviation in the turn on transient, since a factor of 4 in difference is not observed in the gate-drain capacitance.

Conclusion

A digital model of a three level T-type converter was developed based on finite element software, impedance measurements and MOSFET models. The digital representation of the converter was used to perform digital design iterations, before the performance was validated by building a physical demonstrator. The digital model has proven itself useful in the design phase to select model complexity based on transients behaviour, performing targeted attenuations of parasitic resonances and to quantify the gain of design iterations, thus eliminating tedious physical component replacement to optimize physical prototypes. The digital model was in great agreement with the measured response on a μs scale. Comparing measured and simulated waveforms in the nanosecond scale, a discrepancy in dV/dt during turn on was observed. Measured MOSFETs IV-characteristic showed significant differences, capable of explaining the discrepancy between measured and simulated turn on. The measured turn off switching transients were in good agreement with simulation, which was supported by the coherency of the modelled and measured system capacitances. The digital representation of the converter was therefore generally in good agreements with the physical prototype, without corrections and model adjustments. The validity of using the digital model for design iterations was therefore confirmed, without the need of building a physical prototype. If the digital model was desired to be used for accurate simulation of the switching losses, a MOSFET model with an accurate representation of the

transient behaviour is needed.

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Appendix E

Fast and clean switching T-type converter based on SiC MOSFETs for drive Applications

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Fast and clean switching T-type converter based on SiC MOSFETs for drive Applications

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Keywords

High power density systems, Multilevel converters, Silicon Carbide (SiC), Voltage Source Inverters (VSI), Passive filter.

Abstract

The new wide bandgap devices and multilevel topologies make it possible to increase the obtainable power densities for converters. However more complex converters, as a T-type converter, are not optimized for high switching frequencies and rarely evaluated on a converter level. This paper presents a three phase 7.5kW SiC T-type converter optimized for high switching. A THD of 4.6% was obtained with a filter volume of only 60 cm^3 and where only 0.17% of the THD is associated with the switching frequency harmonics.

Introduction

Throughout the history of power electronics, a continuous research focus has been on increasing the efficiency, power density and reducing cost for converter solutions [1]. The increase in efficiency and power density are typically achieved by the advancement within the field of semiconductor technology, enabling the converter to operate with lower semiconductor losses and higher switching frequencies. The lower semiconductor losses are reducing the volume of the heatsink and the higher switching frequency reduces the size of passive filter components [2]. The new wide bandgap devices, introduced in recent years, are therefore of particular interests, as they offer a reduction in switching and conduction losses for the same blocking voltage [3]. For the next generation of converter products, the combination of a T-type converter and wide bandgap devices have received increased focus. The combination is of interests, due to the three output voltage levels and wide bandgap devices enables a

substantial reduction in switching losses, enabling very high switching frequencies. However research publications of converters with a power rating of 10kW show divided views in the optimum selection of a switching frequency, for the same topology and application. For a hardswitched T-type converter utilizing wide bandgap devices the switching frequency ranges from 16 kHz to 160 kHz [4], [5].

Several full SiC T-type converters have been build using discrete package [6],[7] and power modules [8]. The terminals of discrete packages and power modules are introducing a large power and gate loop inductance which limits the obtainable switching performance. The switching speed is limited by the negative gate-source voltage feedback produced by high di/dt and the power loop inductance causing switch over voltage during turn off [9]. The SiC T-type power converters which have been published, are not fully utilizing the advantages of the SiC devices at high switching frequencies. A new optimized power module was developed in our previous work for high switching frequencies and its switching performance was experimentally validated in a double pulse test. The detailed optimization and development of the power module is presented in [10] and will therefore not be covered in detail.

In this paper we utilize the knowledge gained from previous work to build a three phase inverter optimized for high switching frequencies. The T-type converter is build and operated with a switching frequency of 64 kHz, where the power module output current is measured and the harmonic content is quantified. By quantifying the harmonic content of the output filter and its volume, the advantages or disadvantages of increasing the switching frequency beyond the recommend 64 kHz can be clarified and conclusion can be drawn on a system level.

The optimized power module utilizes a Kelvin-Source connection to eliminate the negative gate-source voltage feedback from the high di/dt and the common source inductance. A DC-link snubber is located inside the power module, creating a low impedance path for the high frequency switching currents, improving the switching performance. The internal power loop introduces a parasitic inductance of only 4.3 nH, enabling fast switching without generating hazardous over-voltage for the switch. A switching frequency of 64 kHz was determined using a multi objective pareto optimization algorithm [11]. The Pareto algorithm quantifies efficiency, power density and cost. The algorithm considers a full inverter system including the interaction between power module, heatsink and filter losses and volumes. The algorithm presented the optimum selection of a topology to be a T-type inverter operating with a switching frequency of 64 kHz.

Merits and demerits of T-type converter

A T-type converter is a converter topology with three output voltage levels, as is shown in Figure E.1. The T-type converter utilizes four semiconductor switches to connect the output to one of the DC-link potentials (DC+, MID or DC-). The top and bottom switches blocks the full DC-link voltage and the middle legs switches should withstand half the DC-link voltage.

The T-type converter is reducing the switching losses compared to a half bridge,

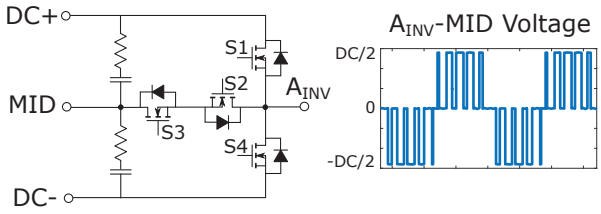

Figure E.1: Single phase, three level T-type topology with output voltage waveform

by reducing the voltage across the active switches to half the DC-link voltage. Furthermore, all semiconductor devices are sharing the switching losses and conduction losses, reducing the thermal impedance from the power module to the heatsink. The disadvantage of a T-type compared to a half bridge converter is the additional switches present and the increased power loop inductance, potentially causing switch over voltage during switching transients.

System simulation and power loss analysis

The power module was optimized in [10] to enable fast switching, as opposed to the power module used in [8]. The fast switching was accomplished by having an internal DC-link snubber in the power module. The semiconductor losses are estimated, using the simulation approach shown in figure E.2, as the switching losses cannot be directly measured by using the currents and voltages at the power module terminals.

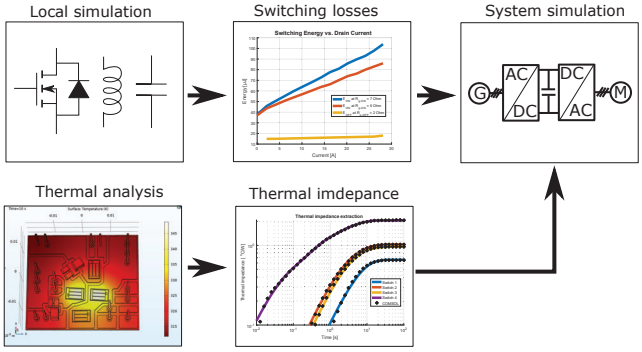

Figure E.2: Flow of information to the system level simulation

The switching losses are estimated using a complex local simulation including layout parasitic, extracted using ANSYS Q3D. The local simulation model and the parasitic extraction was validated in [10]. The parasitic includes inductance, capacitance and mutual couplings from the power module and PCB layouts in combination with the output filter impedance obtained from LCR measurements. The switching losses are derived from the complex local simulations and combined with a thermal network of the power module to a system simulation. The system simulation is capa-

ble of simulating the temperature dependent conduction and switching losses of the semiconductor in steady state operation. The semiconductor power dissipation is simulated under nominal load in figure E.3 . The converter is operating with an output power of 7.5 kW, switching frequency of 64 kHz and a DC-link voltage of 560V. The fundamental output frequency is selected to be 590 Hz, simulating the highest expected output frequency of the inverter, for the specific drive applications considered.

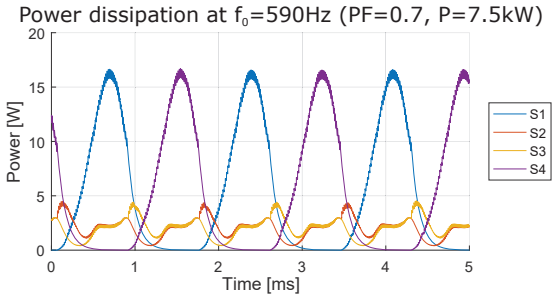

Figure E.3: Semiconductor power dissipation for a single phase power module.

Based on the system simulation, a very low power dissipation per die can be identified. During operation, the predicted semiconductor junction temperature is 38°C which only results in a minor heatsink temperature increase.

Experimental test

The experimental setup consists of three single phase power modules, three individual power routing PCBs with filters, three gate driver PCBs and an interface board connecting the DSP to the control and measurement signals. The three phase inverter with output filter is shown in figure E.4 together with a picture of the power module without housing in figure E.5.

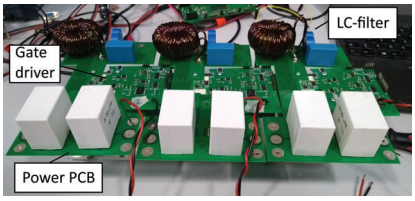

Figure E.4: Three phase, three level T-type SiC inverter including output filter and DC-link.

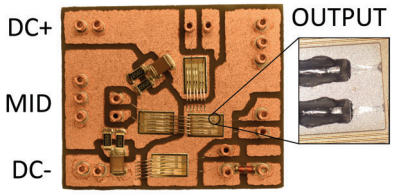

Figure E.5: Optimized power module without housing and terminals.

The focus of the experimental test is full converter operation and filter dynamics at a high switching frequency. The cuttoff frequency of the LC output filter is selected to be at the logarithmic mean of the highest fundamental output frequency (590Hz) and

the switching frequency (64 kHz) resulting in a filter volume per phase of only 60 cm^3. Selecting the cuttoff frequency to be the logarithmic mean ensures a high attenuation of the switching frequency harmonic and a low distortion of the fundamental output frequency.

Results

The experimental results are obtained with a DC-link voltage of 565 V, a switching frequency of 64 kHz and an output current of 10 A rms, but could be scaled to the nominal current of 16 A rms. The output current is limited to 10 A rms, by the allowed power dissipation of the resistive load. To quantify the harmonic content after the filter, the load current was measured. The measurement was performed with a sampling frequency of 50 MHz. The measured load current is shown in figure E.6 with a discrete Fourier transformation (DFT). The DFT is used to extract the harmonic content of the load current.

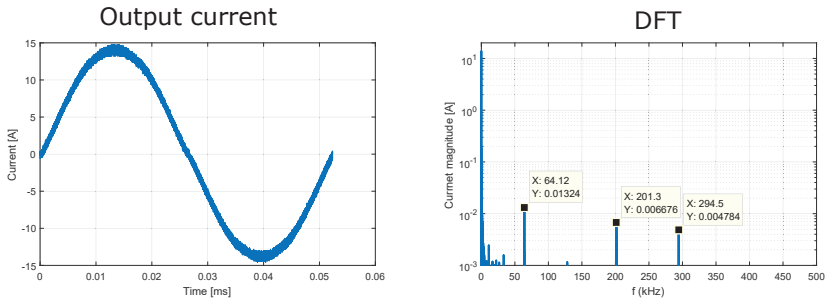

Figure E.6: Output current with a switching frequency of 64 kHz and DC-link voltage of 565V.

The magnitude of the switching harmonic are only 13 mA, 7 mA and 5 mA compared to a fundamental peak current of 14 A. The harmonic distortion contributed from the switching frequency is only 0.17 %, meaning increasing the switching further will have an insignificant reduction of high frequency harmonics. When calculating the THD of the load current, harmonics upto the 50th order of the fundamental frequency were included ($f_{fund} \leqslant 590Hz$). Due to the high switching frequency of 64 kHz, the switching harmonic will not be included when calculating the THD of the output. The total harmonic distortion of the load current was calculated to be 4.6%, with a target limit of 5%. Increasing the switching frequency will not have a substantial impact on the system power density, due to the volume of the output filter being comparable with the volume of the gate driver and power module. The penalty of increasing the switching frequency will be increased switching losses requiring a larger heatsink volume, decreasing the system power density and efficiency. The selection of switching frequency for a T-type converter is therefore validated, by measuring a THD of 4.6% for the load current with only a filter volume of 60 cm^3. After minutes of operation

only a small increase in temperature was observed for the heatsink cooled by natural convection.

Conclusion

A fast and clean switching three phase converter was build in this paper. The three phase T-type power converter was operated at a high switching frequency of 64 kHz with a DC-link voltage of 565V and output current of 10 A rms. The three phase converter demonstrated superior system performance of a T-type converter optimized for high switching frequencies. To evaluate on the selection of switching frequency, the current harmonics of the load were measured. Due to the high switching frequency, the switching frequency harmonics were not considered when calculating the THD. The THD of the load current was 4.6%. A THD of 4.6% was obtained with a filter volume of only 60cm^3 which is comparable to the volume of the power module and gate driver PCB. The filter volume has been substantially reduced by the multilevel topology and high switching frequency, to a point where its contribution is less dominant for a full converter system. Increasing the switching frequency above 64 kHz for a three level inverter in this specific application, will not provide a noticeable positive impact on the overall system power density.

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